

## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

### Programming in C++

Subject Code

:

**06EC661**

IA Marks

:

25

No. of Lecture Hrs/ Week

:

## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

04

Exam Hrs

:

03

Total no. of Lecture Hrs.

:

52

Exam Marks

:

100

# ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

## PART - A

**Unit - 1**

**C++, An Overview:** Getting started, the C++ program, Preprocessor Directives, The Built-In Array Data Type, Dynamic Memory Allocation and Pointers, An Object – based Design, An Object-Oriented Design, An Exception – based Design.

**6 Hours**

**Unit - 2**

**The basic language:** Literal Constant, Variables, Pointer Type, String Types, const Qualifier, Reference Types, the bool type, Enumeration types, Array types. The vector container type.

**6 Hours**

**Unit - 3**

**Operators:** Arithmetic Operators, Equality, Relational and Logical operators, Assignment operators, Increment and Decrement operator, The conditional Operator, Bitwise operator, bitset operations. **Statements:** if, switch, for Loop, while, break, goto, continue statements.

**7 Hours**

**Unit - 4**





## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

### Analog and Mixed Mode VLSI Design

Subject Code

:

**06TE662**

IA Marks

:

25

No. of Lecture Hrs/ Week

## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

:

04

Exam Hrs

:

03

Total no. of Lecture Hrs.

:

52

Exam Marks

:

100

**ELECTIVE – 1 (Group A)**

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

**PART - A**

**Unit - 1 & 2** Impulse Sampling, Sample and Hold, SPICE models for DACs and ADCs, Quantization noise, Spectral density of quantization noise.

**Sampling and Aliasing:** Impulse Sampling, Sample and Hold, SPICE models for DACs and ADCs, Quantization noise, Spectral density of quantization noise.

12 Hours

**Unit - 3 & 4** Effective number of bits Clock jitter, spectral density, Using averaging to improve SNR, Decimating filters for ADCs, Interpolating filters for DACs, Band pass and High pass Sync filters, Using feedback to improve SNR.

**Data Converter SNR:** Effective number of bits Clock jitter, spectral density, Using averaging to improve SNR, Decimating filters for ADCs, Interpolating filters for DACs, Band pass and High pass Sync filters, Using feedback to improve SNR.

14 Hours

**PART - B**

**Unit - 5 & 6** Process flow, capacitors and resistors, SPICE MOSFET models, MOSFET Switch, Delay and Adder elements, Analog circuits – MOSFET Biasing, Op-Amp design, Circuit Noise.

**Sub-Micron CMOS circuit design:** Process flow, capacitors and resistors, SPICE MOSFET models, MOSFET Switch, Delay and Adder elements, Analog circuits – MOSFET Biasing, Op-Amp design, Circuit Noise.





## **ELECTIVE – 1 (Group A)**

Written by Administrator

Saturday, 07 November 2009 07:28 -

---

**1. Mixed simulation signal circuit design (Vol II of CMOS: Circuit design, layout and – R. Jacob Baker, CMOS –), IEEE Press and Wiley Interscience, 2002.**

### **Reference Books:**

**1. Design of Analog CMOS Integrated Circuits – B Razavi, First Edition, McGraw Hill, 2001.**

**2. CMOS Analog Circuit Design – P E Allen and D R Holberg, Second Edition, Oxford University Press, 2002.**

## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

### Random Processes

Subject Code

:

**06EC663**

IA Marks

:

## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

25

No. of Lecture Hrs/ Week

:

04

Exam Hrs

:

03

Total no. of Lecture Hrs.

:

52

Exam Marks

**ELECTIVE – 1 (Group A)**

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

:

100

**PART - A**

**Unit - 1**

**Introduction to PROBABILITY THEORY: Experiments. Sample space, Events, Axioms, Assigning probabilities, Joint and conditional probabilities,. Baye’s Theorem, Independence, Discrete Random Variables, Engg Example.  
7 Hours**

**UNIT - 2**

Random Variables, Distributions, Density Functions: CDF, PDF, Gaussian random variable, Uniform Exponential, Laplace, Gamma, Erlang, Chi-Square, Raleigh, Rician and Cauchy types of random variables.

**7 Hours**

**Unit - 3**



# ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

prediction.

6 Hours

**Unit - 7**

**Random Process:** Definition and characterization, Mathematical tools for studying Random Processes, Stationary and Ergodic Random processes, Properties of ACF.

6 Hours

**Unit - 8**

**Example Processes:** Markov processes, Gaussian Processes, Poisson Processes, Engg application, Computer networks, Telephone networks.

6 Hours

□

**Text Book:**

1. **Probability and random processes: application to Signal processing and communication** – S L Miller and D C Childers Academic Press/ Elsvier 2004.

## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

### Reference Books:

1. **Probability, Random variables and stochastic processes**– Papoullis and S U Pillai: McGraw Hill 2002.
2. **Probability, Random variables and Random signal principles**– Peyton Z Peebles TMH 4<sup>th</sup> Edition 2007.
3. **Probability, random processes and applications** – H Stark and Woods: PHI 2001.

### Adaptive Signal Processing

Subject Code

:

**06EC664**

IA Marks



## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

:

25

No. of Lecture Hrs/ Week

:

04

Exam Hrs

:

03

Total no. of Lecture Hrs.

:

52







## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

### 7 Hours

#### Text Book:□□□□□

□□□

1. Stearns, **Adaptive Signal Processing**– Bernard Widrow and Samuel D., Pearson Education Asia, 2001. E

#### Reference Books:

1. **Adaptive filter Theory**– Simon Haykin, , 4e, Pearson Education Asia, 2002.
2. **Theory and Design of Adaptive Filters** – Jophn R. Treichler C. Richard Johnson, Jr. and Michael G. Larimore, Pearson education/PHI

## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

2002.

### Low Power VLSI Design

Subject Code

:

**06EC665**

IA Marks

:

25

## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

No. of Lecture Hrs/ Week

:

04

Exam Hrs

:

03

Total no. of Lecture Hrs.

:

52

Exam Marks

:

100









## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

### MODERN CONTROL THEORY

Subject Code

:

**06EC666**

IA Marks

:

25

## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

No. of Lecture Hrs/ Week

:

04

Exam Hrs

:

03

Total no. of Lecture Hrs.

:

52

Exam Marks

:

100





# ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

## Unit - 6

Relationship between State Variable and Input-Output Descriptions: Introduction, Input-output Maps from State Models, Output Controllability, Reducibility, State models from Input-Output Maps.

**7 Hours**

## Unit -7

**STABILITY:** Introduction, Stability Concepts and Definitions, Stability of Linear Time- Invariant Systems, Equilibrium Stability of Nonlinear Continuous-Time Autonomous Systems, The Direct Method of Lyapunov and the Linear Continuous-Time Autonomous Systems, Aids to Finding Lyapunov Functions for Nonlinear Continuous-Time Autonomous Systems, Use of Lyapunov Functions to Estimate Transients, The Direct Method of Lyapunov and the Discrete-Time Autonomous Systems.

**6 Hours**

## Unit - 8

## **ELECTIVE – 1 (Group A)**

Written by Administrator

Saturday, 07 November 2009 07:28 -

---

**Model Control:** Introduction, Controllable and Observable Companion Forms, The effect of State Feedback on Controllability and Observability, Pole Placement by State Feedback, Full-Order Observers, Reduced-Order Observers, Deadbeat Control by State Feedback, Deadbeat Observers.

6 Hours

### **Text Book:**

1. **Modern Control System Theory** – M. Gopal :-; 2nd Edition; New Age Int (P) Ltd. 2007

### **Reference Books:**

1. **Modern Control System**– Richard Dorf & Robert Bishop – Pearson Education/ PHI.
2. **Modern Control Engineering** – K. Ogata - - Pearson Education / PHI



## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

### Digital Systems Design Using VHDL

Subject Code

:

**06EC667**

IA Marks

:

25

No. of Lecture Hrs/ Week

:

04

Exam Hrs



# ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

**Introduction:** VHDL description of combinational networks, Modeling flip-flops using VHDL, VHDL models for a multiplexer, Compilation and simulation of VHDL code, Modeling a sequential machine, Variables, Signals and constants, Arrays, VHDL operators, VHDL functions, VHDL procedures, Packages and libraries, VHDL model for a counter.

## 7 Hours

Unit - 2

**Designing With Programmable Logic Devices:** Read-only memories, Programmable logic arrays (PLAs), Programmable array logic (PLAs), Other sequential programmable logic devices (PLDs), Design of a keypad scanner.

## 6 Hours

Unit - 3

**Design Of Networks For Arithmetic Operations:** Design of a serial adder with accumulator, State graphs for control networks, Design of a binary multiplier, Multiplication of signed binary numbers, Design of a binary divider.

## 6 Hours

Unit - 4

**Digital Design with SM Charts:** State machine charts, Derivation of SM charts, Realization of SM charts. Implementation of the dice game, Alternative realization for SM charts using microprogramming, Linked state machines.





## ELECTIVE – 1 (Group A)

Written by Administrator  
Saturday, 07 November 2009 07:28 -

---

### Reference Books:

1. **Fundamentals of Digital Logic Design with VHDL** – Stephen Brown & Zvonko Vranesic, Tata McGraw-Hill, New Delhi, 2<sup>nd</sup> Ed., 2007.

2. **Digital System Design with VHDL** – Mark Zwolinski, 2<sup>nd</sup> Ed, Pearson Education., 2004

3. **Digital electronics and Design with VHDL**– Volnei A Pedroni,. Elsevier Science, 2009