Subject Code		:

IA Marks		: 25

No. of Lecture Hrs/Week		: 04

Exam Hours		: 03

Total no. of Lecture Hrs.		: 52

Exam Marks		: 100

PART - A

Unit - 1

Basic MOS technology: Integrated circuit's era. Enhancement and depletion mode MOS transistors. nMOS fabrication. CMOS fabrication. Thermal aspects of processing. BiCMOS technology. Production of E-beam masks.

4 Hours

MOS Transistor Theory: Introduction, MOS Device Design Equations, The Complementary CMOS Inverter – DC Characteristics, Static Load MOS Inverters, The Differential Inverter, The Transmission Gate, Tristate Inverter.

4 Hours

Unit - 2

Circuit design processes: MOS layers. Stick diagrams. Design rules and layout – lambda-based design and other rules. Examples. Layout diagrams. Symbolic diagrams. Tutorial exercises.

4 Hours

Basic Physical Design of Simple logic gates.

3 Hours

Unit - 3

CMOS logic structures: CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic Cascaded Voltage Switch Logic (CVSL).

6 Hours

Unit - 4

Basic circuit concepts: Sheet resistance. Area capacitances. Capacitance calculations. The delay unit. Inverter delays. Driving capacitive loads. Propagation delays. Wiring capacitances.

4 Hours

Scaling of MOS circuits: Scaling models and factors. Limits on scaling. Limits due to current density and noise.

3 Hours

Unit - 5

CMOS subsystem design: Architectural issues. Switch logic. Gate logic. Design examples – combinational logic. Clocked circuits. Other system considerations.

4 Hours

Clocking Strategies

4 Hours

Unit - 6

CMOS subsystem design processes: General considerations. Process illustration. ALU subsystem. Adders. Multipliers.

6 Hours

Unit - 7

Memory, registers and clock: Timing considerations. Memory elements. Memory cell arrays.

5 Hours

Unit - 8

Testability: Performance parameters. Layout issues. I/O pads. Real estate. System delays. Ground rules for design. Test and testability.

5 Hours

Text Books:

1. **Basic VLSI Design** - Douglas A. Pucknell & Kamran Eshraghian, PHI 3rd Edition (original Edition – 1994), 2005.

2. **Principles of CMOS VLSI Design: A Systems Perspective**, Neil H. E. Weste and K. Eshragian, 2nd edition, Pearson Education (Asia) Pvt. Ltd., 2000.

Reference Books:

1. **Fundamentals of Semiconductor Devices**, M. K. Achuthan and K. N. Bhat, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.

2. **CMOS Digital Integrated Circuits: Analysis and Design**, Sung-Mo Kang & Yusuf Leblebici, 3rd Edition, Tata McGraw-Hill Publishing Company Ltd., New Delhi, 2007.

3. **Analysis and Design of Digital Integrated Circuits** - D.A Hodges, H.G Jackson and R.A Saleh. 3rd Edition, Tata McGraw-Hill Publishing Company Limited, New Delhi, 2007.