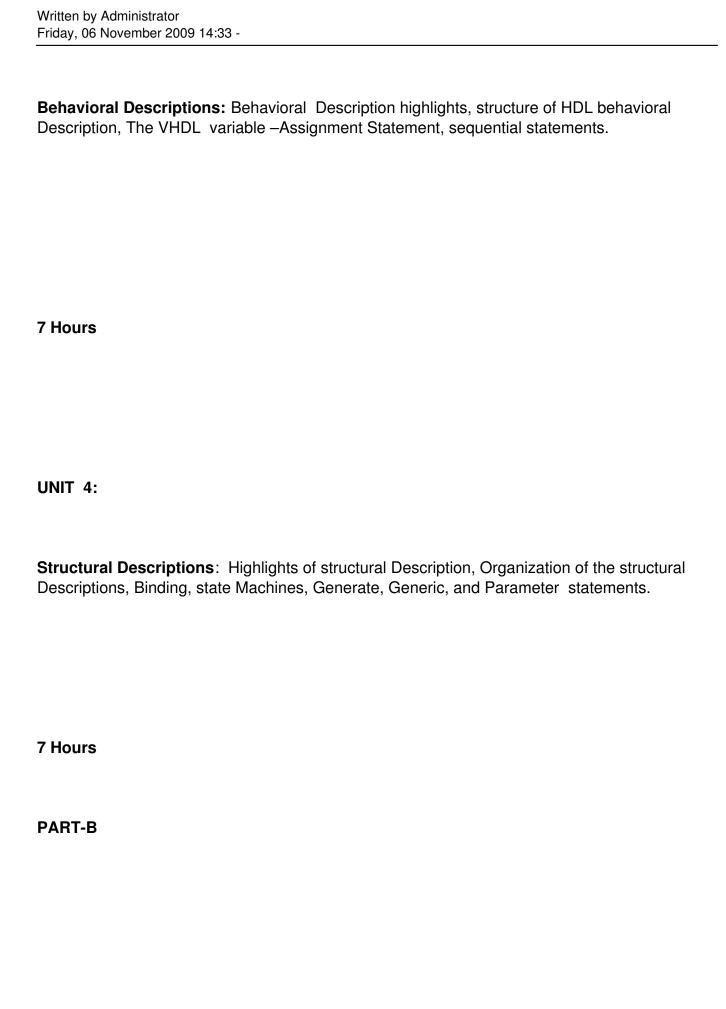
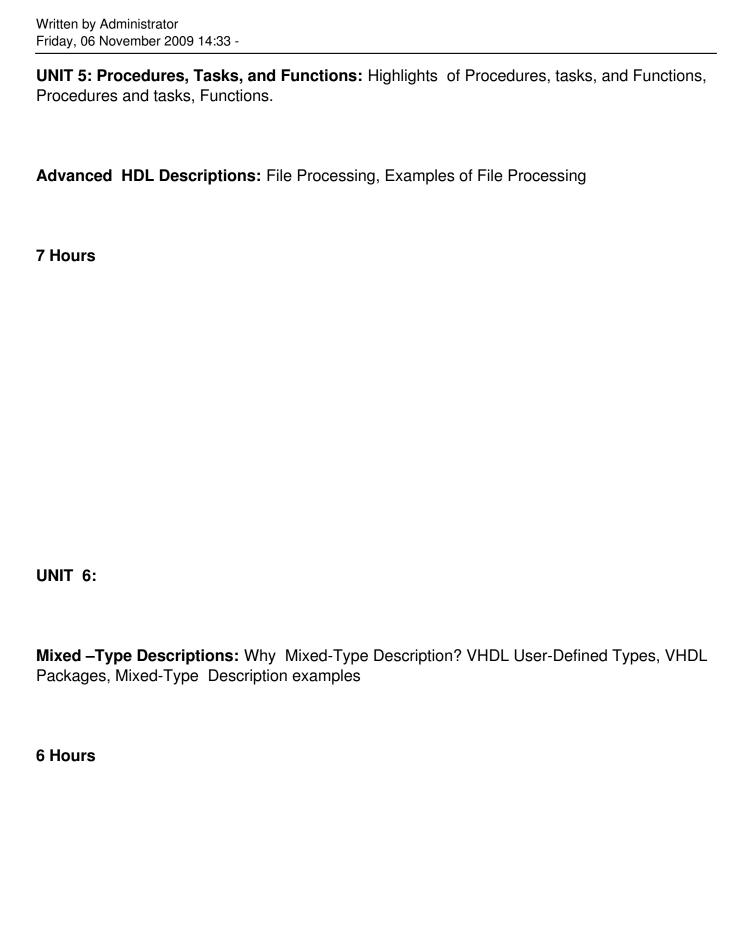
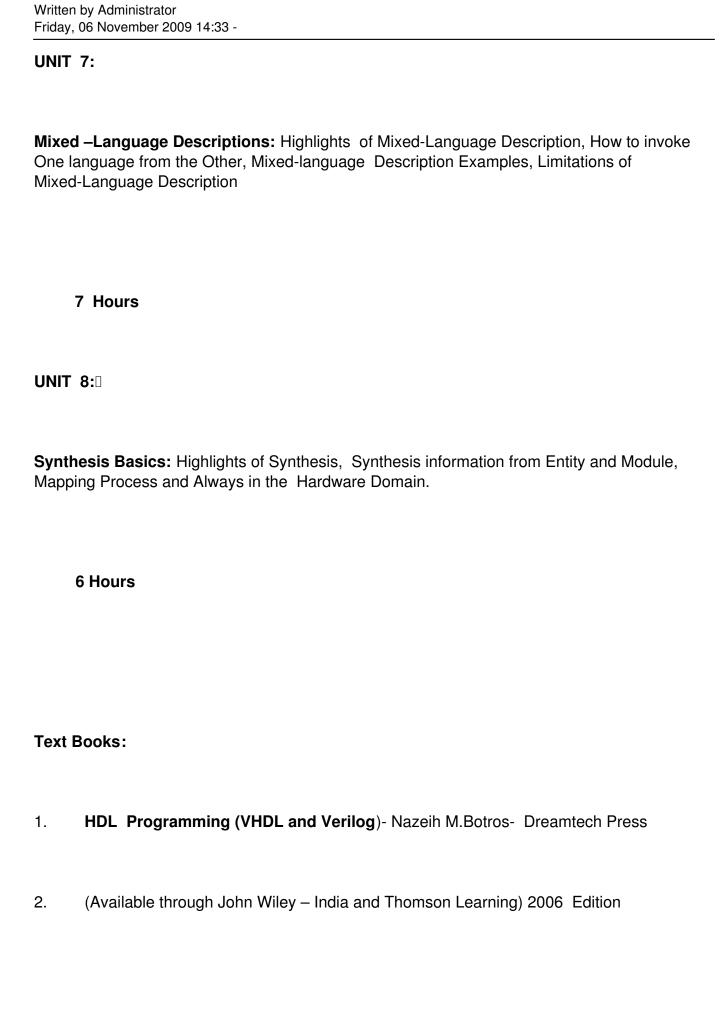
Sub Code  :  O6EC45 IA Marks :  25  Hrs/ Week :  O4	Written by Administrator Friday, 06 November 2009 14:33 -
D6EC45	
06EC45  IA Marks  :  25  Hrs/ Week  :  04	Sub Code
IA Marks  :  25  Hrs/ Week  :  04	
IA Marks  :  25  Hrs/ Week  :  04	
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	Exam Hours

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03	
Total Hrs.	
52	
Exam Marks	
100	

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PART-A
UNIT 1:
□ Introduction: Why HDL?, A Brief History of HDL, Structure of HDL Module, Operators, Data types, Types of Descriptions, simulation and synthesis, Brief comparison of VHDL and Verilog
6 Hours
UNIT 2:
<b>Data –Flow Descriptions:</b> Highlights of Data-Flow Descriptions, Structure of Data-Flow Description, Data Type – Vectors
6 Hours
UNIT 3:







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### **Reference Books:**

- 1. **Verilog HDL** –Samir Palnitkar-Pearson Education
- 2. VHDL -Douglas perry-Tata McGraw-Hill
- 3. **A Verilog HDL Primer** J.Bhaskar BS Publications
- 4. Circuit Design with VHDL-Volnei A.Pedroni-PHI