Subject Code

:

06CS81

IA Marks

:

25

No. of Lecture Hrs./ Week

:

04

Exam Hours

:

03

Total No. of Lecture Hrs.

:

52

Exam Marks

:

100

PART - A

UNIT - 1

FUNDAMENTALS OF COMPUTER DESIGN: Introduction; Classes of computers; Defining computer architecture; Trends in Technology, power in Integrated Circuits and cost; Dependability; Measuring, reporting and summarizing Performance; Quantitative Principles of computer design.

6 hours

UNIT - 2

PIPELINING: Introduction; Pipeline hazards; Implementation of pipeline; What makes pipelining hard to implement?

6 Hours

UNIT - 3

INSTRUCTION –LEVEL PARALLELISM – 1: ILP: Concepts and challenges; Basic Compiler Techniques for exposing ILP; Reducing Branch costs with prediction; Overcoming Data hazards with Dynamic scheduling; Hardware-based speculation.

7 Hours

UNIT - 4

INSTRUCTION –LEVEL PARALLELISM – 2: Exploiting ILP using multiple issue and static scheduling; Exploiting ILP using dynamic scheduling, multiple issue and speculation; Advanced Techniques for instruction delivery and Speculation; The Intel Pentium 4 as example.

7 Hours

PART - B

UNIT - 5

MULTIPROCESSORS AND THREAD –LEVEL PARALLELISM: Introd uction; Symmetric shared-memory architectures; Performance of symmetric shared–memory multiprocessors; Distributed shared memory and directory-based coherence; Basics of synchronization; Models of Memory Consistency.

7 Hours

UNIT - 6

REVIEW OF MEMORY HIERARCHY: Introduction; Cache performance; Cache Optimizations, Virtual memory.

6 Hours

UNIT - 7

MEMORY HIERARCHY DESIGN: Introduction; Advanced optimizations of Cache performance; Memory technology and optimizations; Protection: Virtual memory and virtual machines.

6 Hours

UNIT - 8

HARDWARE AND SOFTWARE FOR VLIW AND EPIC: Introduction: Exploiting Instruction-Level Parallelism Statically; Detecting and Enhancing Loop-Level Parallelism; Scheduling and Structuring Code for Parallelism; Hardware Support for Exposing Parallelism: Predicated Instructions; Hardware Support for Compiler Speculation; The Intel IA-64 Architecture and Itanium Processor; Conclusions.

7 Hours

TEXT BOOK:

1. **Computer Architecture, A Quantitative Approach** – John L. Hennessey and David A. Patterson:

,
4
th

Edition,
Elsevier, 2007.

REFERENCE BOOKS:

1. **Advanced Computer Architecture Parallelism, Scalability** – Kai Hwang:
, Programability

,
Tata Mc Grawhill, 2003.

2. **Parallel Computer Architecture, A Hardware / Software Approach** – David E. Culler, Jaswinder Pal Singh, Anoop

Gupta:, Morgan Kaufman, 1999.