Sub Code

:

06CS33

IA Marks

:

25

Hrs / Week

:

04

Exam Hours

:

03

Total Hrs

:

52

Exam Marks

:

100

PART – A

UNIT 1:

1. Digital Logic: Overview of Basic Gates and Universal Logic Gates, AND-OR-Invert Gates, Positive and Negative Logic, Introduction to HDL

2 Hours

1. Combinational Logic Circuits: Boolean Laws and Theorems, Sum-of-products Method, Truth Table to Karnaugh Map, Pairs, Quads, and Octets, Karnaugh Simplifications, Don't Care Conditions, Product-of-sums Method, Product-of-sums Simplification, Simplification by Quine-McClusky Method, Hazards and Hazard Covers, HDL Implementation Models

5 Hours

UNIT 2:

1. Data-Processing Circuits: Multiplexers, Demultiplexers, 1-of-16 Decoder, BCD-to-Decimal Decoders, Seven-segment Decoders, Encoders, EX-OR gates, Parity

Generators and Checkers, Magnitude Comparator, Read-only memory, Programmable Array Logic, Programmable Logic, Troubleshooting with a Logic Probe, HDL Implementation of Data Processing Circuits

6 Hours

UNIT 3:

1. Arithmetic Circuits: Binary Addition, Binary Subtraction, Unsigned Binary Numbers, Sign-Magnitude Numbers, 2's Complement Representation, 2's Complement Arithmetic, Arithmetic Building Blocks, The Adder-Subtractor, Fast Adder, Arithmetic Logic Unit, Binary Multiplication and Division, Arithmetic Circuits using HDL

6 Hours

UNIT 4:

1. Clocks and Timing Circuits: Clock Waveforms, TTL Clock, Schmitt Trigger, Monostables with Input Logic, Pulse-forming Circuits

2 Hours

1. Flip-Flops: RS Flip-flops, Gated Flip-flops, Edge-triggered RS, D, JK Flip-flops, Flip-flop timing, JK Master-slave Flip-flops, Switch Contact Bounce Circuits, Various Representations of Flip-flops, Analysis of Sequential Circuits, Conversion of Flip-flops – a

synthesis example, HDL implementation of Flip-flop

5 Hours

PART – B

UNIT 5:

1. Registers: Types of Registers, Serial In-Serial Out, Serial In-Parallel Out, Parallel In-Serial Out, Parallel In-Parallel Out, Applications of Shift Registers, Register Implementation in HDL

2 Hours

1. Counters: Asynchronous Counters, Decoding Gates, Synchronous Counters, Changing the Counter Modulus, Decade Counters, Presettable Counters, Counter Design as a Synthesis Problem, A Digital Clock, Counter Design Using HDL

5 Hours

UNIT 6:

1. Design of Sequential Circuit: Model Selection, State Transition Diagram, State Synthesis Table, Design Equations and Circuit Diagram, Implementation using Read Only Memory, Algorithmic State Machine, State Reduction Technique, Analysis of Asynchronous Sequential Circuit, Problems with Asynchronous Sequential Circuits, Design of Asynchronous Sequential Circuit

7 Hours

UNIT 7:

1. D/A Conversion and A/D Conversion: Variable, Resistor Networks, Binary Ladders, D/A Converters, D/A Accuracy and Resolution, A/D Converter-Simultaneous Conversion, A/D Converter-Counter Method, Continuous A/D Conversion, A/D Techniques, Dual-Slope A/D Conversion, A/D Accuracy and Resolution

6 Hours

UNIT 8:

1. Digital Integrated Circuits: Switching Circuits, 7400 TTL, TTL Parameters, TTL Overview, Open-collector Gates, Three-state TTL Devices, External Drive for TTL Loads, TTL Driving External Loads, 74C00 CMOS, CMOS Characteristics, TTL-to-CMOS Interface, CMOS-to TTL Interface

6 Hours

Text Book

1. **Digital Principles and Applications**, Donald P Leach, Albert Paul Malvino & Goutam Saha, 6th Edition, TMH, 2006.

(Chapters 2, 3, 4, 6, Chapter 7-1, 7-2, 7-3, 7-6, 7-7, Chapters 8, 9, 10, 11-1 to 10, 12, 14-1 to 12).

Reference Books

1. **Fundamentals of Digital Logic with Verilog Design**, Stephen Brown, Zvonko Vranesic, TMH, 2006.
2. **Fundamentals of Logic Design**, Charles H. Roth, Jr., 5th Edition, Thomson, 2004.
3. **Digital Systems Principles and Applications**, Ronald J. Tocci, Neal S. Widmer, Gregory L. Moss, 10th Edition, PHI/Pearson Education, 2007.