Written by Administrator Friday, 06 November 2009 05:48 -
Sub Code
06ES32 □
IA Marks
25
Hrs/ Week
:
04
Exam Hours
LAGIII 1 JUUI 3

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03
Total Hrs.
:
52
Exam Marks
100

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PART - A
UNIT 1:
Diode Circuits: Diode Resistance, Diode equivalent circuits, Transition and diffusion capacitance, Reverse recovery time, Load line analysis, Rectifiers, Clippers and clampers. (Chapter 1.6 to 1.14, 2.1 to 2.9)
6 Hours
UNIT 2:
Transistor Biasing : Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased, DC bias with voltage feedback, Miscellaneous bias configurations, Design operations, Transistor switching networks, PNP transistors, Bias stabilization. (Chapter 4.1 to 4.12)
7 Hours
UNIT 3:
Transistor at Low Frequencies: BJT transistor modeling, Hybrid equivalent model, CE Fixed bias configuration, Voltage divider bias, Emitter follower, CB configuration, Collector feedback configuration, Hybrid equivalent model. (Chapter 5.1 to 5.3,

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5.5 to 5.17) 0 00000000000000000000000000000000	000000 00 100000000000000 100000000000
7 Hours	
UNIT 4:	
Transistor Frequency Response : General frequency considerations, low frequency response, Miller effect capacitance, High frequency response, multistage frequency ef (Chapter 9.1 to 9.5, 9.6, 9.8, 9.9)	
6 Hours	
PART – B	
UNIT 5:	

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(a) General Amplifiers: Cascade connections, Cascode connections, Darlington connections. (Chapter 5.19 to 5.27)
3 Hours
(b) Feedback Amplifier: Feedback concept, Feedback connections type, Practical feedback circuits. (Chapter 14.1 to 14.4) 0000000000000000000000000000000000
UNIT 6:
Power Amplifiers : Definitions and amplifier types, series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Amplifier distortions. (Chapter 12.1 to 12.9)
7 Hours

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UNIT 7:
Oscillators: Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (Chapter 14.5 to 14.11)
(BJT version only)
6 Hours
UNIT 8:
FET Amplifiers: FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks. (Chapter 8.1 to 8.13)
7 Harris
7 Hours

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TEXT BOOK:
1. "Electronic Devices and Circuit Theory", Robert L. Boylestad and Louis Nashelsky, PHI/Pearson Eduication. 9^{TH} Edition.
REFERENCE BOOKS:
 'Integrated Electronics', Jacob Millman & Christos C. Halkias, Tata - McGraw Hill, 1991 Edition
2. "Electronic Devices and Circuits", David A. Bell, PHI, 4th Edition, 2004
Question Paper Pattern: Student should answer FIVE full questions out of 8 questions to be set each carrying 20 marks, selecting at least TWO questions
from each part .

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