Seventh semester B.E. Degree Examination, DEC.09/JAN.10 06EC74

DSP ALGORITHMS AND ARCHITECTURE

Time: 3 hrs **Max. Marks:100**

PART-A

1 a. Explain the decimation and interpolation process, with an example.(6M)

b. The sequence x(n)=[0,3,6,9] is interpolated using interpolation sequence bk=[1/3,2/3,1,2/3,1/3] and the interpolation factor of 3. Find the interpolated sequence y(m).

c. Describe the basic features that should be provided in the DSP architecture to be used to implement the Nth order FIR filter,

$Y(n)=\sum_{0}^{n-1} h(i)x(n-i)$; n=0,1,2,…

when x(n) denotes the input sample, y(n) the output sample and h(i) denotes ith filter coefficient.(8M)

2 a. Explain Baugh-Wooley multiplier for signed numbers. Show the multiplication operation for 4 x 4 signed multiplication.(6M)

b. What is meant by circular addressing mode? Write pointer updating algorithm for the circular addressing mode and show different cases that encounter during the updating process of the pointer.(6M)

c. Explain implementation of 8 –tap FIR filter, 1) pipelined using eight MAC units and 2) Parallel using two MAC units. Draw block diagrams.(8M)

3 a. Compare architectural features of TMS320C25 and DSP56000 fixed point digital signal processors.(6M)

b. Write an explanatory note on direct addressing mode of TMS320C54XX processors. Give example.(6M)

c. Describe the operation of the following instructions of TMS320C54XX processors.
1) MPY *AR2-, *AR4+0, B 2) MAC*AR5+, #1234h, A
3) STH A, 1,*AR2 4) SSBX SXM.(8M)

4 a. Explain the following assembler directives of TMS320C54XX processors.(6M)
1) .mmregs 2) .global 3) include ‘xx’ 4) .data 5) .end 6) .bss (6M)

b. Describe Host Port interface and explain its signals.(6M)

c. Write an assembly language program of TMS320C54XX processors to compute the sum of three product terms given by the equation, Y(n)= ho x(n)+h1 x(n-1)+h2 x(n-2) with usual notations. Find y(n) for signed 16 bit data samples and 16 bit constants.(8M)

PART-B

5 a. Determine the value of each of the following 16-bit numbers represented using the given Q-notations : 1) 4400h as Q0 number 2) 4400h as a Q7 number
3) 0.3125 as a Q15 number 4) -0.3125 as a Q15 number.(6M)

b. Write an assembly language program for TMS320C54XX processors to multiply two Q15 numbers to produce Q15 number result.(6M)

c. What is an interpolation filter? Explain the implementation of digital interpolation using FIR filter and poly phase subfilter.(8M)

6 a. Determine the following for a 128-point FFT computation: 1) number of stages

2) number of butterflies in each stage 3) number of butterflies needed for the entire computation 4) number of butterflies that need no twiddle factors 5) number of butterflies that requires real twiddle factors 6) number of butterflies that require complex twiddle factors.(6M)

b. Explain, how scaling prevents overflow conditions in the butterfly computation.(6M)

c. With the help of implementation structure, explain the FFT algorithm for DIT-FFT computation on TMS 320C54XX processors, Use 1/4 as scale factor for all butterflies.(8M)

7 a. Explain a data memory system with address range 000800h-000FFFh for a C5416 processor using 2Kx8 SRAM memory chips.(6M)

b. Explain an interface between an A/D converter and the TMS320C54XX processor in the programmed I/O mode.(6M)

c. Describe DMA with respect to TMS320C54XX processors.(8M)

8 a. Explain PCM3002 CODEC, with the help of a neat block diagram.(6M)

b. Explain DSP-based biotelemetry receiver system, with the help of a block schematic diagram.(6M)

c. With the help of a block diagram, explain the image compression and reconstruction using JPEG encoder and decoder.(8M)

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