NEW SCHEME

EC662

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Sixth Semester B.E. Degree Examination, July/August 2005

Electronics & Communication / Telecommunication Engineering

DSP Architectutre

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Why decimation and interpolation is necessary in digital signal processing? What is its effect in frequency domain? **(8 Marks)**

(b) Consider a 4 point sequence $x(n)$ with samples $x(n) = \{2, \underset{\uparrow}{3}, 2, 1\}$. Find the DFT of the 12-point sequence described by $y(n) = \{x(n), x(n), x(n)\}$. Use interpolation or decimation principle whichever is applicable. **(12 Marks)**

2. (a) Draw the Braun multiplier structure to multiply two unsigned numbers,

$A = A_4A_3A_2A_1A_0$

$B = B_4B_3B_2B_1B_0$

What is the propagation delay if each adder introduces 1 unit delay? How many adders are required. **(10 Marks)**

(b) Identify the addressing modes of the operands in each of the following instructions (AR stands for address register)

$ADD \ \# \ 1234h$

$ADD \ 1234h$

$ADD \ * \ AR+$

$ADD \ offsetaddr-, \ * \ AR$ **(4 Marks)**

(c) List the major architectural features used in a digital signal processor to achieve high speed of program execution. **(6 Marks)**

3. (a) What are special addressing modes and why they are required in DSP? Explain two such addressing modes, with examples. **(10 Marks)**

(b) With a neat block diagram explain the functions of an address generation unit of DSP architecture. **(10 Marks)**

4. (a) Briefly describe the following instructions of TMS 320C54 XX processors with an example.

i) $MACR*AR5 + ,*AR6+, A, B$

ii) $RPT \ Smem$

iii) $RPTB$

iv) $BANZ$

v) $LD, Smem, 16, DST$ **(10 Marks)**

Contd.... 2

(b) Write a TMS32054xx program to compute the sum of three product terms given by the equation :

$$y(n) = h_0x(n) + h_1x(n-1) + h_2x(n-3)$$

using the MAC instruction, where $h_0, h_1, \& h_2$ are the filter coefficients stored in program memory locations starting at h. $x(n)$, $x(n-1)$ and $x(n-2)$ are data samples stored in data memory locations starting at x.$y(n)$ is to be saved in location $y(low\ 16\ bits)$ and $y+1(high\ 16\ bits)$. (10 Marks)

5. (a) What is the significance of Q - notation in DSP. Explain with examples. (7 Marks)

(b) Determine the value of each of the following 16-bit numbers represented using the given Q - notation :

i) 4400 h as a Q0 number

ii) 4400 h as a Q15 number

iii) 4400 h as a Q7 number (3 Marks)

(c) What is an interpolation filter. Explain the need of an interpolation and decimation filter in DSP. (10 Marks)

6. (a) What is an adaptive filter. Explain how such a filter can be implemented in DSP. (10 Marks)

(b) Implement the IIR filter represented by the following difference equation on the TMS320C54 xx. Assume that Q15 notation is used to represent the values of coefficients and QO to represent the signal samples.

$$y(n) = b(0)x(n) + b(1)x(n-1) + a(0)y(n-1) + a(1)y(n-2) + a(2)y(n-3)$$ (10 Marks)

7. (a) An 8-point FFT is to be implemented using DIT-FFT method on TMS 320 C54xx. Give the FFT implementation structure and also explain the algorithm that computes the output of each stage. (10 Marks)

(b) Determine the following for a 128-point FFT computation.

i) Number of stages

ii) Number of butterflies in each stage

iii) Number of butterflies needed for the entire computation

iv) Number of butterflies that need no twiddle factors. (4 Marks)

(c) Design an interface to connect a $64K \times 16$ flash memory to a TMS320C54xx device. The processor address bus is $A0 - A15$. (6 Marks)

8. (a) With a neat block diagram explain the functioning of a multichannel buffered serial port (McBSP) of C54 xx. (7 Marks)

(b) What is a CODEC? With a neat block diagram explain the working of PCM3002 CODEC. (6 Marks)

(c) With a neat block diagram explain the implementation of DSP based Biotelemetry receiver. (7 Marks)

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NEW SCHEME

Sixth Semester B.E. Degree Examination, July 2006
Electronics and Communication Engineering
DSP Architecture

Time: 3 hrs.] [Max. Marks:100

Note: *1. Answer any FIVE full questions.*

1 a. With a neat block diagram explain the components of a DSP system. What are the disadvantages of a digital signal processing and how are they overcome. **(07 Marks)**

b. Compute the power spectral density (PSD) of a sequence $x(n) = n[u(n) - u(n-4)]$ using DIT-FFT method. Plot the PSD. **(08 Marks)**

c. Explain major architectural features of programmable digital signal processors. **(05 Marks)**

2 a. Why special addressing modes are provided in digital signal processors. With examples signal processors. With examples explain such addressing modes. **(10 Marks)**

b. Consider the implementation of an 8-tap FIR filter given by

$$y(n) = \sum_{i=0}^{7} h(i)x(n-i)$$

Explain pipelined implementation of this filter using :
i) eight MACS ii) parallel implementation using two MACS. **(10 Marks)**

3 a. Draw the functional diagram of the multiplier / adder unit of TMS320C54xx processor is classified into various categories based on their functions. Give examples. **(07 Marks)**

b. Explain how the instruction set of TMS320C54xx processor is classified into various categories based on their functions. Give examples. **(08 Marks)**

c. Describe the operation of the following instructions:
i) MPY 13, B ii) MPY #01234, A iii) MPY *AR2-, *AR4+0, B
iv) MAC *AR5+, #1234, A v) MAC *AR3-, *AR4+, B, A. **(05 Marks)**

4 a. What is the significance of Q-notation in DSP? What values are represented by the 16-bit fixed point number N=4000 hexadecimal in Q15 and Q7 notations? **(05 Marks)**

b. Explain the implementation of PID controller using DSP. **(07 Marks)**

c. Explain how matrix multiplication algorithm can be implemented using TMS320C54xx. **(08 Marks)**

5 a. With necessary equations explain how a basic DIT-FFT butterfly in-place computation structure is implemented in TMS320C54xx. **(10 Marks)**

b. Explain how scaling prevents overflow conditions in the butterfly computation. Derive the optimum scaling factor for the DIT-FFT butterfly. **(10 Marks)**

6 a. Design a data memory system with address range 000800h – 000FFFh for a C5416 processor. Use 2KX8 SRAM memory chips. Give the schematic of the interface. **(10 Marks)**

b. How does the interrupt handling in the C54xx DSP differ for a software and a hardware interrupt. **(10 Marks)**

7 a. What is Multichannel Buffered Serial Port (McBSP)? Explain various handshaking and control signals of McBSP with a neat block diagram. **(10 Marks)**

b. Draw the block diagram of JPEG encoder and decoder and also explain how JPEG encoding and decoding is implemented in DSP. **(10 Marks)**

8 Explain briefly:

a. A speech processing system. **(06 Marks)**

b. Interpolation filters. **(07 Marks)**

c. Host Port Interface (HPI). **(07 Marks)**

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NEW SCHEME

Sixth Semester B.E. Degree Examination, Dec.06 / Jan.07
EC / TE
DSP Architecture

Time: 3 hrs.] [Max. Marks:100

Note: ***1. Answer any FIVE full questions.***

1 a. What is a digital signal processor? What is the criterion for choosing the sampling frequency in such a system? **(08 Marks)**

b. What is meant by decimation and interpolation? Explain how aliasing is overcome in interpolation with the help of time and frequency domain diagrams. **(06 Marks)**

c. A two stage decimator is used to decrease the sampling rate from 500 KHz to 12.5 KHz. The decimation factors for the first and second stages of decimators are 10 and 4 respectively. Draw the block diagram of the complete decimator. What should be the cutoff frequency of the second stage anti-aliasing filter? **(06 Marks)**

2 a. Write briefly about the Analysis and Design tool used in the digital signal processing. **(06 Marks)**

b. Write a program in MATLAB to compute linear convolution of the following two sequences:
$x(n) = \{ 1, 2, 3, 4 \}$ and $h(n) = \{ 3, 2, 1 \}$ **(04 Marks)**

c. What is the difference between a microcoded program control and a hardwired program control? Why is the latter preferred in the DSP device? **(04 Marks)**

d. What do you mean by 'On – Chip memory' as applied to a digital signal processor architecture? Describe briefly the important issues related to the design of such a memory. **(06 Marks)**

3 a. What is a barrel shifter in a DSP device and why it is used? Explain how a 4 bit, shift-right barrel shifter can be implemented. **(06 Marks)**

b. Explain guard bits in a MAC unit of a DSP device. Consider a MAC unit whose inputs are 24-bit numbers. How many guard bits should be provided if 512 products have to be added in the accumulator to prevent overflow condition? What is the overall size of the accumulator required? **(10 Marks)**

c. Explain following directives used by the assembler to compile assembly language program in TMS 320C54xx DSP device:
i) .mmregs
ii) .include"xx"
iii) .data
iv) .text **(04 Marks)**

4 a. Explain briefly the major architectural features used in a DSP device to a achieve high speed of program execution. **(06 Marks)**

Contd...2

4 b. Show the pipeline operation of the following sequence of instructions if the initial value of AR3 is 80 and the values stored in the memory locations 80, 81, 82 are 1, 2, 3 respectively.

```
LD    *AR3+, A
ADD   #1000h, A
STL   A, *AR3+
```

(08 Marks)

c. A digital Signal processor has a circular buffer with the start and end addresses as 0200h and 0310h. What is the circular buffer size? What would be the new values of address pointer of the above buffer if, in the course of address computation, it gets updated to i) 0336h ii) 0192h. **(06 Marks)**

5 a. Explain Q-notation used in digital signal processing algorithm implementation. What is the range of values of a 16 bit number in Q15 representation? **(06 Marks)**

b. What values are represented by 16 bit number N = 3000h in Q15 and Q7 notations? **(04 Marks)**

c. What do you mean by 2-D signal processing? How is memory organized for implementation of matrix multiplication algorithm of a 3x4 matrix with a 4x3 matrix in TMS 320C54xx? **(10 Marks)**

6 a. What minimum size FFT must be used to compute a DFT of 220 points in Radix-2 algorithm? Determine the number of butterfly structures needed for this algorithm and thereby determine number of complex multiplications and additions needed? **(08 Marks)**

b. What do you mean by bit-reversed index-generation and how it is implemented in TMS 320C54xx DSP device? **(06 Marks)**

c. How are interrupts handled in TMS 320C54xx DSP device? Explain briefly interrupt handling with the help of a flowchart. **(06 Marks)**

7 a. Explain briefly the building blocks of a PCM 3002 CODEC circuit. **(08 Marks)**

b. Why are decimation and interpolation filters used in the above codec circuit? **(04 Marks)**

c. Explain Multichannel Buffered Serial Port circuit in TMS 320C54xx device with the help of a block diagram. How many such units are there in this type of DSP device? **(08 Marks)**

8 a. What do you understand by a DSP based Biotelemetry Receiver? **(06 Marks)**

b. How is ECG signal processing done for heart rate determination decoding PPM signal? **(06 Marks)**

c. Give the overview of JPEG algorithm in image processing with the help of a block diagram. **(08 Marks)**

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NEW SCHEME

Sixth Semester B.E. Degree Examination, July 2007
EC / TE
DSP - Architecture

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Explain in brief with a neat block diagram the issues to be considered in designing and implementing a DSP system. **(06 Marks)**

b. Explain in brief major features of Programmable Digital Signal Processors. **(04 Marks)**

c. Explain in brief the following in relation to the speed issues in DSP Architecture i) Harvard Architecture ii) Parallelism iii) Pipelining. **(10 Marks)**

2 a. Explain in brief with neat block diagram the methods of sampling rate conversions in DSP techniques. What is its effect in frequency domain? **(08 Marks)**

b. Determine the low pass filter cut-off frequency that must be used to decimate to reduce the sampling rate from 8 kHz to 4 kHz. **(04 Marks)**

c. An FIR filter is described by the equation

$Y(n) = h(o).x(n) + h(1).x(n-1) + \text{--------} + h(N-1).x(n-(N-1))$ with usual notations. With this example, explain why conventional processors do not perform well on DSP based applications. **(08 Marks)**

3 a. What are special addressing modes and why they are required in DSP? Explain two such addressing modes with examples. **(10 Marks)**

b. Briefly describe the following instructions of TMS320C54XX processors with an example. **(10 Marks)**

i) MACD ii) RPTB pmad iii) BANZ iv) MPY xmem, Ymem, dst. v) BACC

4 a. By means of a figure the pipeline operation of the following sequence of instructions if the initial values of AR1, AR3, A are 84, 81, 1 and the values stored in the memory locations 81, 82, 83, 84 are 2, 3, 4, 6. Also provide the values of registers AR3, AR1, T and Accumulator A after completion of each cycle. **(08 Marks)**

```
ADD * AR3+, A
 LD  * AR1 +, T
MPY *AR3 +, B
ADD  B, A
```

b. What is an adaptive filter? Explain how such filter can be implemented in DSP – in brief. **(08 Marks)**

c. A DSP has a circular buffer with start and end addresses as $O200_h$ and $O20F_h$ respectively. What would be the new values of the address pointer of the buffer, if in the course of address computation, it gets updated to i) $O212_h$ ii) $O1FC_h$. **(10 Marks)**

Contd...2

5 a. What is the significance of Q-notation in DSP? Explain with examples. **(07 Marks)**

b. Write a TMS320C54XX program that illustrates the multiplication of two "Q15" numbers to produce Q15 result. **(03 Marks)**

c. Explain with a neat block diagram the implementation of P.I.D. controller. **(10 Marks)**

6 a. Design a data-memory system with address range 000800_h – $000FFF_h$ for a C5416 processor. Use 2K×8 SRAM memory chips. **(04 Marks)**

b. Write the structure of an 8-point DITFFT implementation. Take scale factor for all butterflies as ¼. **(06 Marks)**

c. Write a program segment that implements matrix multiplication. **(10 Marks)**

7 a. What is CODEC? With a neat block diagram, explain the working of PCM3002 CODEC. **(06 Marks)**

b. Explain with a neat block diagram JPEG Encoder and JPEG Decoder. **(04 Marks)**

c. Explain in brief how interrupt handling is done in TMS320C54XX series DSP. **(10 Marks)**

8 Write short notes on :

a. 4×4 Braun Multiplier

b. Bit – reversal index generation.

c. Host Port Interface

d. Synchronous Serial Interface.

e. Speech Processing System. **(20 Marks)**

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EC662

Sixth Semester B.E. Degree Examination, Dec. 07 / Jan. 08
DSP Architecture

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. With block diagram, explain the scheme of a digital signal processing system. **(06 Marks)**

b. If x(n) = (1,2,3,1), compute and plot power spectral density. **(06 Marks)**

c. Draw and explain Braun multiplier structure to multiply two, 4-bit unsigned numbers A and B. **(08 Marks)**

2 a. Draw MAC unit used in DSP. Explain any two methods used to avoid overflow and under flow. **(08 Marks)**

b. Describe the addressing modes provided in the architecture of DSP to implement real time signal processing algorithms. **(09 Marks)**

c. Identify the addressing modes of the operands in each of the following instruction and their operation :
i) ADD # 1234h ii) ADD *AR+ iii) ADD 1234h. **(03 Marks)**

3 a. An Eight tap FIR filter is given by $y(n) = \sum_{i=0}^{7} h(i)x(n-i)$. Implement using i) Single MAC unit and ii) Parallel implementation using two MAC units. Compare the pmethods. **(10 Marks)**

b. Describe the operation of the following of the following instructions of TMS 320 C54XX processors.
i) MAC * AR5 +, # 1234h,B ii) MPY * AR2-,*AR4 + 0,B iii) MAS *AR3-,*AR4+,B,A
iv) ADDS *AR2-,B v) SUBS *AR2-,B **(05 Marks)**

c. A DSP has a circular buffer with the start and end addresses as 0200h and 020Fh, respectively. What would be the new values of the address pointer of the buffer if, in the course of address computation, it gets updated to i) 0212h ii) 01FCh. **(05 Marks)**

4 a. Write a program to compute the sum of three product terms given by the equation y(n) = h(0)x(n)+h(1)x(n-1)+h(2)x(n-2). Using the indirect addressing mode where h(0),h(1)and h(2) are the filter coefficients stored in program memory locations starting at h, x(n),x(n-1) and x(n-2)are the data samples stored in data memory locations starting at 310h,311h and 312h, and y(n) is to be saved in location y(low 16 bits) and y+1(high 16 bits). **(08 Marks)**

b. Name data addressing modes of TMS 320C54XX processor. With block diagram and example explain the direct addressing mode of TMS320C54XX processor. **(05 Marks)**

c. By means of figure, explain the pipe line operation of TMS320 C54XX processors. **(07 Marks)**

5 a. What is Q-notation? Compute the values represented by the 16 bit fixed point number N=4000h in the Q15 and Q7 notations. **(06 Marks)**

b. Explain how a digital decimation filter can be implemented for a given decimation factor. **(08 Marks)**

c. Explain how a matrix multiplication algorithm can be implemented using TMS320C54XX **(06 Marks)**

6 a. An 8-point FFT is to be implemented using DIT FFT method on TMS 320 C54XX. Give the FFT implementation structure and also explain the algorithm that computes the output of each stage. **(10 Marks)**

b. Explain how a scaling prevents overflow conditions in the butterfly computation. Derive the optimum scaling factor for the DIT-FFT butterfly. **(10 Marks)**

7 a. Design a data memory system with address range 000800h-000FFFh for C5416 processor. Use 2kX8SRAM memory chips. Give the schematic of interface. **(08 Marks)**

b. What is a multichannel buffered serial port (McBSP) with block diagram? Explain various handshaking and control signals of McBSP. **(09 Marks)**

c. How does DMA help in increasing the processing speed of a DSP processor? **(03 Marks)**

8 a. What is CODEC? With a neat block diagram explain the working of PCM3002 CODEC. **(06 Marks)**

b. With block diagram explain the implementation of DSP based biotelemetry receiver. **(06 Marks)**

c. Draw the block diagram of JPEG encoder and decoder and explain how these are implemented in DSP. **(08 Marks)**

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EC662

Sixth Semester B.E. Degree Examination, Dec. 07 / Jan. 08
DSP Architecture

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. With block diagram, explain the scheme of a digital signal processing system. **(06 Marks)**

b. If x(n) = (1,2,3,1), compute and plot power spectral density. **(06 Marks)**

c. Draw and explain Braun multiplier structure to multiply two, 4-bit unsigned numbers A and B. **(08 Marks)**

2 a. Draw MAC unit used in DSP. Explain any two methods used to avoid overflow and under flow. **(08 Marks)**

b. Describe the addressing modes provided in the architecture of DSP to implement real time signal processing algorithms. **(09 Marks)**

c. Identify the addressing modes of the operands in each of the following instruction and their operation :
i) ADD # 1234h ii) ADD *AR+ iii) ADD 1234h. **(03 Marks)**

3 a. An Eight tap FIR filter is given by $y(n) = \sum_{i=0}^{7} h(i)x(n-i)$. Implement using
i) Single MAC unit and ii) Parallel implementation using two MAC units. Compare the pmethods. **(10 Marks)**

b. Describe the operation of the following of the following instructions of TMS 320 C54XX processors.
i) MAC * AR5 +, # 1234h,B ii) MPY * AR2-,*AR4 + 0,B iii) MAS *AR3-,*AR4+,B,A
iv) ADDS *AR2-,B v) SUBS *AR2-,B **(05 Marks)**

c. A DSP has a circular buffer with the start and end addresses as 0200h and 020Fh, respectively. What would be the new values of the address pointer of the buffer if, in the course of address computation, it gets updated to i) 0212h ii) 01FCh. **(05 Marks)**

4 a. Write a program to compute the sum of three product terms given by the equation y(n) = h(0)x(n)+h(1)x(n-1)+h(2)x(n-2). Using the indirect addressing mode where h(0),h(1)and h(2) are the filter coefficients stored in program memory locations starting at h, x(n),x(n-1) and x(n-2)are the data samples stored in data memory locations starting at 310h,311h and 312h, and y(n) is to be saved in location y(low 16 bits) and y+1(high 16 bits). **(08 Marks)**

b. Name data addressing modes of TMS 320C54XX processor. With block diagram and example explain the direct addressing mode of TMS320C54XX processor. **(05 Marks)**

c. By means of figure, explain the pipe line operation of TMS320 C54XX processors. **(07 Marks)**

5 a. What is Q-notation? Compute the values represented by the 16 bit fixed point number N=4000h in the Q15 and Q7 notations. **(06 Marks)**

b. Explain how a digital decimation filter can be implemented for a given decimation factor. **(08 Marks)**

c. Explain how a matrix multiplication algorithm can be implemented using TMS320C54XX **(06 Marks)**

6 a. An 8-point FFT is to be implemented using DIT FFT method on TMS 320 C54XX. Give the FFT implementation structure and also explain the algorithm that computes the output of each stage. **(10 Marks)**

b. Explain how a scaling prevents overflow conditions in the butterfly computation. Derive the optimum scaling factor for the DIT-FFT butterfly. **(10 Marks)**

7 a. Design a data memory system with address range 000800h-000FFFh for C5416 processor. Use 2kX8SRAM memory chips. Give the schematic of interface. **(08 Marks)**

b. What is a multichannel buffered serial port (McBSP) with block diagram? Explain various handshaking and control signals of McBSP. **(09 Marks)**

c. How does DMA help in increasing the processing speed of a DSP processor? **(03 Marks)**

8 a. What is CODEC? With a neat block diagram explain the working of PCM3002 CODEC. **(06 Marks)**

b. With block diagram explain the implementation of DSP based biotelemetry receiver. **(06 Marks)**

c. Draw the block diagram of JPEG encoder and decoder and explain how these are implemented in DSP. **(08 Marks)**

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EC662

Sixth Semester B.E. Degree Examination, June / July 08
DSP Architecture

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Explain about decimation. Briefly explain how the decimated sequence is obtained. **(06 Marks)**

b. The sequence x(n) = {0, 4, 8, 12, 16} is interpolated using interpolation sequence $b_k = \{1/4, 2/4, 3/4, 1, 3/4, 2/4, 1/4\}$ and the interpolation factor is 4. Find the interpolated sequence y(m). **(10 Marks)**

c. Write a MATLAB program to compute linear convolution of the following two sequences. x(n) = {2, 1, -2, 2} and h(n) = {3, 1, 2, -1}. **(04 Marks)**

2 a. Draw and explain the 3× 3 Braun multiplier structure. What is the total propagation delay if each adder introduces 1.5 unit delay? **(10 Marks)**

b. Identify the addressing modes of the operands in each of the following instructions and their operations. i) ADD B ii) ADD # 2233h iii) ADD 2233h iv) ADD* addrreg, off setreg + **(05 Marks)**

c. A sum of 512 products are to be summed up in a MAC using pipelined operation. The inputs to the Mac are 16-bit numbers. The MAC execution time is 50ns. Find i) What will be the total time required to complete the operation? ii) How many guard bits should be provided for the accumulator to prevent the overflow condition? **(05 Marks)**

3 a. Briefly explain the special addressing modes. **(08 Marks)**

b. Draw the block diagram of parallel implementation of an 8-tap FIR filter using two MAC units and compare it with pipelined implementation. **(06 Marks)**

c. With the help of functional diagram, explain about the Multiplier / Adder unit of TMS320C54XX processors. **(06 Marks)**

4 a. Describe the operation of the following instructions of TMS 320C54XX processors.
i) MPY # 2314, A ii) MAC * AR5- , * AR6+, A, B **(03 Marks)**

b. Explain what is accomplished by the following instruction sequence.
RPT # 3 ; MAC * AR3 - , * AR2+, A **(03 Marks)**

c. Write TMS320C54XX program to compute the sum of three product terms given by the equation. y(n) = h(0) x(n) + h(1) x(n-1) + h(2) x(n-2), using direct addressing mode.
Where h(0), h(1) and h(2) are stored in data memory locations starting at location h and x(n), x(n-1) and x(n-2) are stored in data memory locations starting at location x. y(n) is saved in data memory locations y (low 16 bits) and y+1 (high 16 bits). **(09 Marks)**

d. Assume that the register AR4 with contents 2040h is selected as the pointer for the circular buffer. Let BK = 50 h. Determine start and end addresses for the buffer. What will be the contents of the register AR4 after the execution of the instruction? i) LD*AR4 + 0%, A ; ii) *AR4 – OB , if the contents of AR0 is 0035h? **(05 Marks)**

5 a. What values are represented by the 16-bit fixed point number N = 5736h in Q0, Q6, Q10 and Q15 notations. **(10 Marks)**

b. Explain how the IIR filter can be implemented using TMS320C54XX processor (only algorithm is needed). **(10 Marks)**

6 a. Explain how the Bit-reversed index generation can be done in 8 point DIT FFT. **(04 Marks)**

b. With the help of signal flow graph, explain about the FFT implementation algorithm for 8-point DIT-FFT on the TMS320C54XX . Scale factor for all butterflies = ¼. **(06 Marks)**

c. Interface an 8k × 16 program ROM to the 'C5416 DSP in the address range 7FE000h – 7FFFFFh. **(10 Marks)**

7 a. Explain the Multi channel buffered serial port (M_C BSP) with the help of block diagram. **(10 Marks)**

b. Draw the block diagram of the PCM3002 CODEC and explain about it. **(10 Marks)**

8 a. With the help of block diagram, explain the memory interface for TMS320C5416 processor. Also draw the timing diagram for a read-read- write sequence of operations. **(10 Marks)**

b. With the help of block diagram, explain the Image compression and Reconstruction using JPEG encoder and decoder. **(10 Marks)**