 (3 Nos 6 pages) EC/TC **EC5T3**

Reg. No. | | | | | | | | | | |

Fifth Semester B.E. Degree Examination, July/August 2002

Electronics & Communication Engineering

Microprocessor

Time: 3 hrs.] [Max.Marks : 100

Note: ***Answer any FIVE full questions.***

1. (a) With a block schematic, describe the functions of the general purpose, special purpose and flag register of 8085. (10 Marks)

   (b) Define machine cycle and instruction cycle. (2 Marks)

   (c) Describe how the address and data lines are demultiplexed? Also write the logic circuit to generate the control signals of 8085. (8 Marks)

2. (a) What are the functions of the following pins of 8085? i) RST 7.5 ii) $\overline{INTA}$ and iii) Ready. (3 Marks)

   (b) Describe the addressing modes of 8085 with an example. (5 Marks)

   (c) Write an 8085 ALP to subtract two BCD numbers using 10's complement arithmetic. (8 Marks)

   (d) What happens if the clock frequency of 8085 is below $500KH_z$? (4 Marks)

3. (a) Explain the operation performed by 8085 when the following instructions are executed. i)SBB C ii)RRC iii) LDAX B iv) XTHL. (8 Marks)

   (b) Is it possible to check AC flag status of 8085? Explain. (4 Marks)

   (c) Write an 8085 ALP to convert an 8-bit binary number into its equivalent BCD value. (8 Marks)

4. (a) Calculate the count value to implement a subroutine for generating 2 msecond delay using a register pair. Assume the clock frequency of 8085 as 3 MH_z. Write an 8085 ALP to downcount from $85_{10} to 25_{10}$. Use the delay routine to display the count value on the data filed. (10 Marks)

   (b) The number of T-states for JNZ is 10/7. What is its significance? (2 Marks)

   (c) Explain how CALL instruction is executed by 8085, indicating the operations in all the machine cycles. (5 Marks)

   (d) The only logical instruction group which sets AC flag is logical AND (ANA/ANI), where as AC flag is cleared by the other logical instructions. Why? (3 Marks)

5. (a) Distinguish between

   i) Memory mapped I/O and I/O mapped I/O

   ii) Read only memory and Read/Write memory. (4 Marks)

   (b) Interface 8K x 8 EPROM and 16K x 8 R/W M to 8085 without shadows. Also write the memory map for the purpose. Starting address of EPROM should be 0000 H. (8 Marks)

Contd.... 2

(c) Write the timing diagram for the instruction

i) IN 42 H

ii) STA 2050. (8 Marks)

6. (a) Describe an input and an output port with addresses 80 and 81 H respectively to connect a linear key board and a 7-segment unit respectively. (6 Marks)

(b) Describe mode 0 and BSR mode of 8255 PPI. (6 Marks)

(c) Write an 8085 ALP to read a data byte using serial input line of 8085. (8 Marks)

7. (a) Interface an 8251 USART to 8085 and write an 8085 ALP to transmit the message GOOD LUCK onto a CRT terminal. (8 Marks)

(b) Describe the operations of (i) 8259 PIC and (ii) 8257 DMA. (12 Marks)

8. (a) Explain the control word format and modes of operations of 8253 timer. Generate a delay of 0.5 second using mode 0 of 8253. (10 Marks)

(b) Describe the internal architecture of 8279 KB display controller. Interface a 3×8 keyboard matrix and 6 common cathode 7 segment display units to 8085 using 8279. (10 Marks)

** * **

EC5T3

Reg. No.

ifth Semester B.E. Degree Examination, January/February 2003

Electronics & Communication Engineering

Microprocessor

Time: 3 hrs.] [Max.Marks : 100

Note: ***Answer any FIVE full questions.***

1. (a) Explain with the help of a neat block diagram, the internal architecture of 8085, detailing all the signals. (10 Marks)

   (b) Give the Flag register structure of 8085 and explain its contents. (5 Marks)

   (c) Draw neatly the Opcode fetch timing diagram and give description of each signal. (5 Marks)

2. (a) Write an assembly language program to generate Fibonocci numbers (0, 1, 1, 2, 3, 5 .... N) upto N where N is also a Fibonocci numbers. Include comments. (10 Marks)

   (b) Explain the function of the following instructions.

   i) XCHG ii) SPHL iii) XTHL iv) NOP v) PUSHPSW. (5 Marks)

   (c) Differentiate between JUMP, CALL and RSTn instructions in their execution. (5 Marks)

3. (a) Write an assembly language program to multiply and divide two 8 bit numbers. The results should be outputed with one second delay. Assume a clock frequency of 3 MHz. (10 Marks)

   (b) A micro computer has 8 K EPROM and two 4 kRAM memories. Using linear decoding give a circuit to interface these memories with 8085. Assume suitable starting addresses. (10 Marks)

4. (a) Differentiate between 8155 and 8255 programmable peripheral interfaces. (5 Marks)

   (b) Differentiate between :

   i) I/O mapped I/O ii) Memory mapped I/O. (5 Marks)

   (c) Interface using 8255 PPI and digital to analog converter to generate a stair case wave form with a step size of 0.5ms and 0.5v. Write the program with comments. (10 Marks)

5. (a) Using only SID and SOD pins explain how you can establish a serial communication between two distant points. (5 Marks)

   (b) Differentiate between synchronous and asynchronous serial data transfer of information. (5 Marks)

   (c) Explain the internal architecture of 8251 with the help of a neat block diagram. (10 Marks)

Contd.... 2

6. (a) How many interrupts are present in a 8085 MPU and what are their ty and differences? (5 Mark

(b) Explain how two 8259s can be cascaded to achieve more interrupts. (5 Marks)

(c) Give the internal architecture of 8257 DMA controller and explain the functions of various blocks. (10 Marks)

7. (a) Give the block diagram of 8279 key board/ Display controller and explain the functions of

i) SCAN lines ii) Blank display. (10 Marks)

(b) Explain all the modes of 8253 programmable Interval timer with the help of timing diagrams. (10 Marks)

8. (a) What are the aspects of 8275 CRT controller makes it needed for interfacing a CRT with MPU? Explain. (8 Marks)

(b) What are

i) Light pen input ii) Row buffers (80 × 8)

iii) Character generator ROM iv) Raster timing and control. (12 Marks)

** * **

EC5T3

USN | | | | | | | | | | |

ifth Semester B.E. Degree Examination, January/February 2004

Electronics & Communication Engineering

Microprocessor

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. 8085 instruction set is provided on request.

1. (a) What are addressing modes used in the following instructions? Explain
MVI M, 03FH
IN 4
PUSH B
RET

(8 Marks)

(b) Index addressing is not available directly in 8085! What could be done in lieu of this? Explain with an example. (6 Marks)

(c) If the CALL and RET instructions were not provided in 8085, could it be possible to write subroutine for this microprocessor? If so how? (6 Marks)

2. (a) Why do you think it is necessary for the 8085 to have TWO status lines S_1 and S_0 How much time would be required in 8085 to save all GPRS and all status registers? (4 Marks)

(b) What is multiplexing? Why is it used in 8085? Discuss the pros and cons of it on the working of the microprocessor. (6 Marks)

(c) Discuss the method adopted for devising the Op-codes of 8085. Device the op codes for
MVI B, BYTE
MOV B,C

(10 Marks)

3. (a) For the delay routine below, write an expression that gives a total delay time of the routine as a function of N and the state time T. Determine the value of N required for a 1 ms delay. Assume an 8085 A processor with a 6.144 MHz crystal.

```
Delay  :  LXI B, N
LOOP   :  DCX B
          MOV A,B
          ORA C
          JNZ : LOOP
```

Write an expression for the delay routine that gives the total delay time as a function of the loop control variable, N, the state time, T and the number of wait states, W. (10 Marks)

(b) If the CALL and RET instructions were not provided in 8085, could it be possible to write subroutines for this microprocessor? If so, how? Explain with an example. (5 Marks)

(c) Write an ALP to simulate the Decimal adjust after BCD addition without using DAA instruction of 8085. (5 Marks)

Contd.... 2

4. (a) Compute the time required to multiply two natural numbers X and Y 8085. Do the same for division of X by Y? Use suitable program for ti purpose. (14 Marks)

   (b) Construct at least one example to show that the program length decreases if GPRs are available in a μP. Use the 8085 instruction set as a guide line. (6 Marks)

5. (a) Write a subroutine that adds two 4 digit BCD numbers. Assume that the operands are in register pairs BC and DE before the subroutine is called. The subroutine should have the least significant 4 digits of BCD result in register pair DE and the value of the carry in the least significant 4 bits of register C. (8 Marks)

   (b) Why is that in the I/O mapped mode, only 256 input and 256 output devices can be addressed? (5 Marks)

   (c) Interface 4K bytes of EPROM and 6k bytes of RAM to 8085. Use 2716 (2K X 8) and 2142 (K X 4) chips. (7 Marks)

6. (a) How is the device priority determined in hardware polling? (6 Marks)

   (b) While a device is being serviced, suppose that another device interrupts, if hardware polling is used, when will the interrupt request for this device be served? (5 Marks)

   (c) Generate a square wave with ON time=OFF time=0.5 ms, using 8155. Assume clock frequency = 1 MHz, and address of CR, port A, port B, port C, timer and timer MSB are F8H through FDH. (9 Marks)

7. (a) Write a subroutine, SCAN, that, when called, scans a 16-key keypad (in 4 X 4 matrix). The subroutine should first direct whether any switch is closed, and if not, return immediately. If one or more switches are closed, the subroutine should return with the code for the switch or switches in the accumulator. (8 Marks)

   (b) Compare hardware and software polling techniques for device identification upon interrupt. Use circuit cost and device identification time as criteria. (8 Marks)

   (c) Discuss the read and write timings of the memory when interfaced with the microprocessor. (4 Marks)

8. (a) Explain the architecture of various functional blocks of 8259 (interrupt controller). (7 Marks)

   (b) Explain the initialization and operation command words for 8259. (4 Marks)

   (c) Design a frequency counter using an 8253 and 8085 A. (9 Marks)

** * **

EC5T3

USN | | | | | | | | | | |

Fifth Semester B.E. Degree Examination, July/August 2004

Electronics & Communication Engineering

Microprocessor

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Draw the internal architecture of 8085 and explailn. Clearly indicate the importance of various registers. (10 Marks)

   (b) Draw : i) Opcode fetch machine cycle

   ii) Memory write machine cycle

   iii) I/O read machine cycle and explain. (10 Marks)

2. (a) Interface 8K × 8 ROM using 2716 and $4K \times 8RAM$ using 2114IC's. Use suitable decoder. Assume the starting addresses for ROM and RAM as 0000H and COOOH respectively. (10 Marks)

   (b) Write an assembly language program to find nC_r of 8 bit number. Write subroutine to find factorial at a number and use it to calculate nC_r. (10 Marks)

3. (a) With suitable programming example clearly explain passing the parameter through regs, through memory and through stack. (10 Marks)

   (b) Assuming $T = 325.5ns$, write a program segment which generates a delay of $0.5sec$. (5 Marks)

   (c) Write an assembly language program to count number of 1's and 0's present in a hex byte present at 2100H memory location. Store number of 1^s at 2101H and number of O^s at 2102H memory locations. (5 Marks)

4. (a) Design a decoder which decodes $IO/\overline{m}, \overline{RD}$ and $\overline{WR}$ into two active low signals $\overline{MERD}$, $\overline{MEWR}$, $\overline{IORD}$ and $\overline{IOWR}$. (6 Marks)

   (b) Differentiate between memory mapped I/O and isolated I/O. (6 Marks)

   (c) Interface two input ports at addresses FFFO and FFF1H and two output ports at addresses 9000H and 9001 H using memory mapped I/O. Indicate the assumptions made if any. (8 Marks)

5. (a) Interface a single 8255 to 8085 starting with the address OCH. Also write a program segment to do following.

   i) Define Port A and B as input and Port C as output port mode O.

   ii) Read the data from Ports A and B, add them and send the 2's complement of the result to Port C. (10 Marks)

   (b) With suitable block diagram, control word; explain model input and output operations of 8255. (10 Marks)

Contd.... 2

6. (a) Explain with diagram serial synchronous and asynchronous data formats 8251. (6 Marks)

(b) Write a program to transmit 8 bit data through SOD pin starting with MSB. The data is stored at address 1A00H. (8 Marks)

(c) Briefly explain the timer of 8155. (6 Marks)

7. (a) Write a 8085 program to generate a square wave of 100 Hz from the source of 10 kHz using 8253 / 8254. Clearly indicate the assumption made if any. (8 Marks)

(b) Draw interval block diagram of CRT controller and explain. (8 Marks)

(c) Differentiate between Nkey roll-over and 2key lock out. (4 Marks)

8. Write notes on :

(a) Cascading of 8259 (7 Marks)

(b) DMA and its importance (7 Marks)

(c) Limitation of 8085 instruction set (6 Marks)

** * **

EE5T4

USN | | | | | | | | | | |

fth Semester B.E. Degree Examination, January/February 2005

Electrical & Electronics Engineering

(Old Scheme)

Microprocessors

Time: 3 hrs.] [Max.Marks : 100

Note: ***Answer any FIVE full questions.***
Write flow charts wherever necessary.

1. (a) Write the pin out diagram of the 8085 microprocessor and the signals and chip specifications. (10 Marks)

(b) List the various registers in 8085 and describe their applications and the flags. (8 Marks)

(c) What is the difference between a microprocessor and microcomputer? (2 Marks)

2. (a) Explain the terms T-state and machine cycle. Explain the timing diagram for execution of instruction MOV B,C. (10 Marks)

(b) What are the basis on which the instruction set of 8085 microprocessor can be classified? Explain the classification giving atleast 2 examples for each. (10 Marks)

3. (a) Write a program to (6 Marks)

i) Clear the contents of accumulator

ii) Add 47 H

iii) Subtract 92 H

iv) Add 64H

v) Display the results after subtracting 92 H and after adding 64 H. Show the flag status after each step. Specify the answer you would expect at the output port. Specify the reason for clearing the accumulator in step 1.

(b) A data set containing fifteen readings is stored in consecutive memory locations starting from memory 9000 H. Write a program to

i) Check whether the readings are positive or negative

ii) Reject all negative readings

iii) Add all positive readings

iv) Output FF to port 1 at any time when the sum exceeds eight bits to indicate overload, otherwise display the sum.

Note : MSB is used to indicate whether the number is positive or negative.

Draw the flow chart also. (14 Marks)

4. (a) Explain the instructions RIM, SIM. Mention their importance. How do you interpret the contents of the accumulator? (8 Marks)

Contd.... 2

(b) Write subroutine to obtain 250 msec (milliseconds) delay. Specify the count to be loaded in the DE register pair. Write the flow chart. Show all calculations. Assume that the crystal connected to the processor is 4 MHz. Specify the necessary precautions taken when writing the subroutine. **(12 Marks)**

5. (a) Read the following program and answer the queries. **(10 Marks)**

Line No.	Mnemonics
1	LXI SP, 0800
2	LXI B , 2055
3	LXI H , 22FF
4	LXI D , 2090
5	PUSH H
6	PUSH B
7	MOV A , L
:	:
↓	↓
20	POP H

i) What is stored in the stack pointer register after the execution of line 1?

ii) What is the memory location of the stack where the first data byte wire be stored?

iii) What is stored in memory location 07FEH when line 5 is executed (ie after PUSH H)?

iv) After the execution of line 6 what is the contents of SP (stack pointer)? **(10 Marks)**

(b) A set of ten packed BCD numbers is stored in memory location starting at 9050 H.

Write a program with a subroutine to add these numbers in BCD. If a carry is generated, save it in register B, and adjust it for BCD. The final sum will be less than 9999_{BCD} **(10 Marks)**

6. (a) What are interrupts? How are they classified? With a neat figure explain the various 8085 interrupts and their vector locations. **(10 Marks)**

(b) What are the schemes in which I/O devices can be interfaced with the microprocessor? Compare the schemes. **(6 Marks)**

(c) What is an assembler? What are the various assembler directives? State their purpose. **(4 Marks)**

7. (a) Write the block diagram of 8255 and explain the control section signals. **(8 Marks)**

(b) What are the modes of operation of 8255? Explain the control word format for the modes. **(12 Marks)**

8. (a) What are the different modes of operation of 8253? Explain. **(10 Marks)**

(b) List the major components of the 8259 interrupt controller and explain their functions. **(10 Marks)**

** * **

USN | | | | | | | | | | |

Fifth Semester B.E. Degree Examination, July/August 2005

Electronics & Communication Engineering

Old Scheme

Microprocessor

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. 8085 OP-Code sheet is provided on request.

1. (a) What is the function of status register ? Describe the function of other registers of 8085. **(6 Marks)**

(b) Draw the functional block diagram of 8085 and explain each block in brief. **(8 Marks)**

(c) Name the different phases involved in the execution process of an instruction. Explain. **(6 Marks)**

2. (a) Describe the functions of the following pins of 8085

i) READY ii) ALE iii) $IO/\overline{M}$ iv) HOLD v) RESET **(5 Marks)**

(b) What is a subroutine ? How it is useful ? Explain the use of stack in CAL and RETURN instructions. **(6 Marks)**

(c) Compare the following pairs of instructions with their addressing mode, affected flags and the results.

i) XTHL and SPHL

ii) SUB B and CMP B

iii) MVIA, OO and XRA A **(9 Marks)**

3. (a) Write an ALP to generate a delay of 0.4 sec, if the crystal frequency is 5MHz. **(9 Marks)**

(b) Write a circuit diagram to achieve

i) Power on reset circuit

ii) Wait state gen genarator circuit **(6 Marks)**

(c) Explain stack operation in detail. **(5 Marks)**

4. (a) Sketch and explain the timing diagram for the instruction

i) MOV M, A ii) DCRM **(10 Marks)**

(b) Differentiate between I/O mapped I/O and memory mapped I/O. **(5 Marks)**

(c) How do you enhance the number of interrupt levels at INTR pin of 8085 ? Explain . **(5 Marks)**

5. (a) How is the device priority determined in hardware polling ? Explain. **(5 Marks)**

(b) Write an ALP to transfer 10 data bytes stored in memory location XX20H. Serially via SOD pin of 8085. **(9 Marks)**

Contd.... 2

(c) Explain interrupt driven I/O technique. How 8085 responds to INTR interrupt ? **(6 Marks)**

6. (a) Illustrate different modes of operation of 8253/54. **(10 Marks)**

(b) Design a monostable multi vibrator to obtain a pulse of width 5 milli second with 8253 using an external clock of $100KHz$. **(10 Marks)**

7. (a) Explain the features and operation of 8257 DMA controller using block schematic. **(10 Marks)**

(b) Draw and explain command and mode word formats of 8251. **(10 Marks)**

8. (a) List the features of 8270. **(5 Marks)**

(b) Explain the terms 2 - key lockout and N-key lockover. **(5 Marks)**

(c) Interface 8×4 key matrix key board to 8085 using 8255. Write an ALP to initialise 8255 and to read the key board. **(10 Marks)**

** * **

NEW SCHEME

CS56

USN | | | | | | | | | | |

Fifth Semester B.E. Degree Examination, January/February 2005

Computer Science Engineering

Advanced Microprocessors

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. All questions carry equal marks.

1. (a) Describe the memory interfacing signals of intel 386 and 486 processors and illustrate their use in a 32 bit bus system.

   Why is it that the bank select signals are used only with memory write operation and not with memory read operation? (10 Marks)

   (b) Indicate the different pins of the 8279 (keyboard/ display controller) chip and explain their functions. (10 Marks)

2. (a) With a block diagram, explain the 8254 timer chip and briefly describe its modes of operation. (10 Marks)

   (b) How would you use the 8254 chip, with a transistor bridge, to control the direction and speed of rotation of a small d.c. motor? (10 Marks)

3. (a) Explain the complete operation of the hardware interrupt on the Intel 86 family of processors, from the instant the hardware interrupt request is made by a peripheral to the instant the processor branches to the service routine. (10 Marks)

   (b) Briefly describe a printer interface to an 8088 system using an auxiliary 8088 processor for handling the printer and the spooler. (10 Marks)

4. (a) Describe the MFM and the RLL methods of data recording in hard discs. (10 Marks)

   (b) What are the built in constants which can be directly loaded into the 80×87 floating point processor? (4 Marks)

   (c) Describe the various transcendental function that can be directly generated by the 80×87 processor? (6 Marks)

5. (a) Explain the basics of the MMX and XMM technologies and their use. (10 Marks)

   (b) With respect to the PCI bus, explain:

   i) the PCI commands

   ii) configuration space

   iii) PCI BIOS (10 Marks)

Contd.... 2

6. (a) In respect of the USb (Universal Serial Bus) explain the following :

i) The NRZI coding used

ii) Use of bit stuffing

iii) The data packets used

iv) The CRC used. (10 Marks)

(b) Explain the various steps to be taken before the Intel 386 and later processor can be taken from the real mode to the protected mode. (10 Marks)

7. (a) Describe the operation of the internal cache of the 486 processor. (10 Marks)

(b) Distinguish between burst cycle and the non burst cycle of the 80486 processor with appropriate timing diagrams. (10 Marks)

8. (a) With suitable diagrams, describe the internal structure of the Pentium Pro processor. (10 Marks)

(b) Describe the characteristic features of the RISC processors and bring out their advantages over the CISC processors. (10 Marks)

** * **