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06EC63

Sixth Semester B.E. Degree Examination, May/June 2010
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the characteristics and typical errors associated with sample and hold circuit. **(10 Marks)**

b. Briefly explain the ADC specifications. **(05 Marks)**

c. Find the resolution of DAC, if the output voltage is desired to change in 1 mV increments while using a reference voltage of 4V. **(05 Marks)**

2 a. Explain qualitatively the architecture and working of charge scaling DACs. **(10 Marks)**

b. Design a 3-bit charge scaling DAC and find the value of output voltage for $D_2D_1D_0$ = 100 and 011. Assume V_{ref} = 5V, C = 0.5 PF. **(05 Marks)**

c. Briefly explain the architecture & working of a pipeline digital to analog coverter. **(05 Marks)**

3 a. Explain the architecture and working of a flash ADC. **(08 Marks)**

b. If a 10-bit flash ADC is designed, determine maximum offset voltage of comparators which will make INL less than ½ LSB. Assume that resister string is perfectly matched and V_{REF} = 4V. **(04 Marks)**

c. Briefly explain the block diagram of a 2-step flash ADC and its working. **(08 Marks)**

4 a. Explain qualitatively preamplification and decision circuits of a CMOS comparator unit. Draw their CMOS circuits. **(10 Marks)**

b. Explain the principle of an analog multiplier. **(05 Marks)**

c. Briefly explain CMOS analog multiplier with the help of a circuit diagram. **(05 Marks)**

PART – B

5 a. Define SNR, effective number of bits and clock jitter in mixed signal circuits qualitatively. **(08 Marks)**

b. Explain the principle of averaging to improve SNR, in mixed signal circuits. **(06 Marks)**

c. Briefly explain the role of decimating filters in ADCs. **(06 Marks)**

6 a. With a neat process flow diagram, explain submicron CMOS technology and bring out the differences as compared to CMOS technology. **(10 Marks)**

b. Explain how capacitor and resister elements are fabricated in submicron technology. **(07 Marks)**

c. Explain MOSFET as a switch. **(03 Marks)**

7 a. What are delay elements? Explain how they are realized using pass transistors, inverters and C^2MOS and TSPC circuits. **(10 Marks)**

b. Realize a 4-bit pipelined adder using latches and explain its operation. **(05 Marks)**

c. Implement full adder using dynamic logic and explain. **(05 Marks)**

8 a. Consider a small signal amplification of a floating current source shown in Fig.Q8(A). Assuming NMOS cascade o/p resistance is labeled R_{ncas}, what is the small signal resistance scan by test voltage V_{test}? **(10 Marks)**

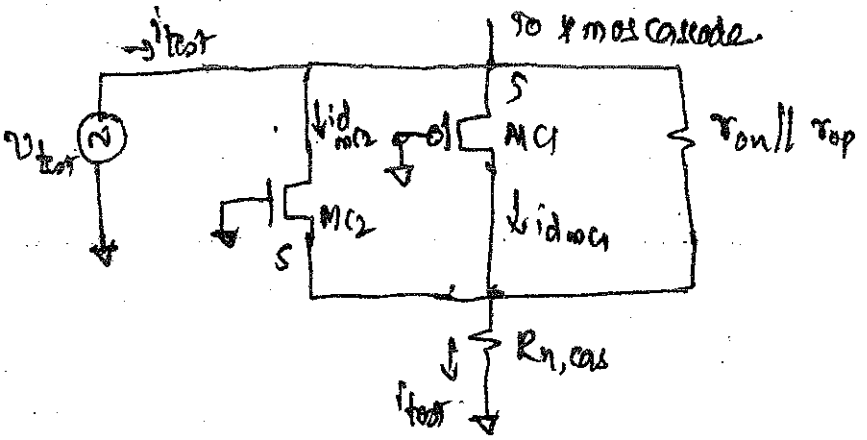

Fig.Q8(A)

b. Explain with the help of circuit diagrams, the technique of making the flow rate concern in the design of op amp. **(10 Marks)**

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