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06EC63

Sixth Semester BE Degree Examination, Dec.09-Jan.10
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: *1. Answer any FIVE full questions, selecting at least TWO questions from each part.*
2. Standard notations are used.
3. Missing data be suitably assumed.

PART – A

1 a. Define Resolution, INL, DNL and V_{FS} for a DAC. (06 Marks)

b. Find the maximum DNL and INL in LSBs of a 3 bit DAC which has the following characteristics. Check if it is monotonic. (10 Marks)

Digital input	000	001	010	011	100	101	110	111
Analog output	0 V	0.625 V	1.5625 V	2.0 V	2.5 V	3.125 V	3.4375 V	4.375 V

c. Find the maximum resolution of an ADC which can use the S/H circuit with maximum sampling error of 0.628 mV while maintaining a sampling error less than 1/2 LSB Vref = 5V.

2 a. Discuss the issues involved in mixed signal circuit layout. (04 Marks)

b. Describe the simple resistor string DAC, problem associated with it and how is it overcome by use of a binary switch array. (10 Marks)

3 a. Describe the pipelined ADC with a neat diagram. (10 Marks)

b. For an 8 bit pipelined ADC, all the amplifiers had a gain of 2.1 v/v instead of 2v/v. If V_{in} = 3V and V_{ref} = 5V, what would be the resulting digital output, assuming other components are ideal. (08 Marks)

c. For a 4 bit successive approximation ADC with V_{ref} = 5V, V_{in} = 1V, find the output digital code. Assume a dual slope successive approximation ADC. For each clock cycle, give the output of the SAR, V_{aut} and the final output. (06 Marks)

4 a. Discuss the advantages and disadvantages of using a dual slope over a single slope ADC. (06 Marks)

b. Draw the CMOS analog multiplier and explain its working. (07 Marks)

c. Discuss transient response, propagation delay and minimum slewrate of a comparator. (07 Marks)

PART – B

5 a. Develop an expression for effective number of bits in terms of the measured SNR if the input wave has a peak amplitude of 30% of V_{ref}. (07 Marks)

b. With a neat block diagram, describe the accumlate and dump circuit for decimation and averaging. (07 Marks)

c. Sketch the block level circuit diagram for an fs/4 digital resonator. (06 Marks)

6 a. With relevant diagrams, describe the CMOS process flow, for devices with L_{min} <0.35 μm. (10 Marks)

b. Describe with a neat diagram, the conceptual layout and actual layout of an R-2R resistor string with minimum area and also discuss the problem of laying out metal over the resistive material. (10 Marks)

7 a. Sketch the implementation of a synchronous up/down counter and discuss its operation. (07 Marks)

b. Draw the 4 bit pipelined adder and describe how it operates. (08 Marks)

c. Draw the positive edge triggered delay using clocked CMOS logic. (05 Marks)

8 a. Illustrate how a pushpull output stage is biased with a floating current source. (07 Marks)

b. Infer that, to minimize the input referred noise, the gain of the first stage of the amplifier should be large in a cascade of amplifiers. (06 Marks)

c. Discuss circuit noise in an opamp. (07 Marks)

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06EC63

Sixth Semester B.E. Degree Examination, June-July 2009
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. State the reasons for the pedestal error, droop aperture error and sampling error. **(08 Marks)**

b. State and explain specifications of ADC. **(12 Marks)**

2 a. An 8 bit resistor string DAC was fabricated with a nominal resistor value of 1 kΩ. If the process was able to provide matching of resistors to within 1%, find maximum INL and DNL of the converter. Assume $V_{REF} = 5V$. **(06 Marks)**

b. Explain generic (unweighted) current steering DAC and discuss the related mismatch errors. **(08 Marks)**

c. Design a 4 bit charge scaling DAC using a split array. Assume that $V_{REF} = 5V$ and that C = 0.5 pF. Draw the equivalent circuit for D = 0001 and 0010 and determine the value of the output voltage. **(06 Marks)**

3 a. Explain the principle of single slope ADC and the problems associated with it. **(10 Marks)**

b. Draw the block diagram for 4 bit successive approximation ADC with $V_{REF} = 5V$. Explain the same. Trace the output at various stages for $V_{in} = 3.7V$. **(10 Marks)**

4 a. Explain the purpose of each stage of a voltage comparator. Also explain the working of 1st stage. **(10 Marks)**

b. Show that multiplying quad acts as multiplier when all the MOSFETs in the multiplying quad have the same threshold voltage. **(10 Marks)**

PART – B

5 a. Determine the ideal SNR of a 8 bit data converter with averaging of 20 outputs. **(04 Marks)**

b. Draw the circuit arrangement used for decimation and averaging and explain the same. Determine the transfer function of the same. **(10 Marks)**

c. Bring out the principle of interpolation. **(06 Marks)**

6 a. Describe CMOS process flow with neat sketches. **(10 Marks)**

b. Explain how MOSFET behaves as a capacitor. Also explain floating MOS capacitor. **(10 Marks)**

7 a. Estimate the high-to-low and low-to-high delays in the circuits shown in figure Q7 (a). **(08 Marks)**

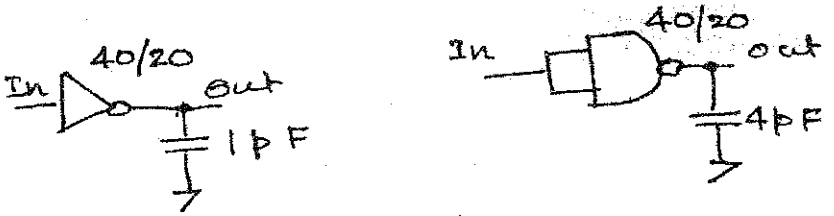

Fig. Q7 (a)

b. Draw the arrangement for 4 bit pipelined adder and full adder bit implemented using dynamic logic. **(06 Marks)**

c. Explain the working of simple delay element using pass transistor and CMOS inverter. **(06 Marks)**

8 a. Explain the limitations of inverter at the output of OPAMP, with the help of its transf curve. How is it overcome? **(07 Mark**

b. Consider the AC small signal simplification of floating current source as in figure Q8 (b Assuming NMOS cascade output resistance is labeled R_{NCOS}, what is the small signa resistance as seen by the test voltage V_{test}? **(07 Mark**

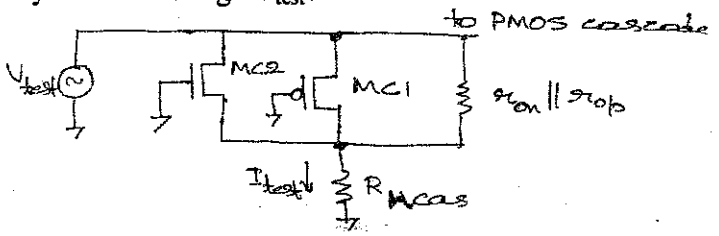

Fig. Q8 (b)

c. Determine time constant of OPAMP with unity gain frequency of 100 MHz. Assume that al the outputs is fed back to the input. Also determine the settling time for 0.1% settlin accuracy. **(06 Marks**

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