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06EC63

Sixth Semester B.E. Degree Examination, December 2010
Analog and Mixed Mode VLSI Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART - A

1 a. With reference to a DAC describe :
i) Resolution ii) LSB iii) DNL iv) INL v) V_{FS} vi) Dynamic range.
Find the value of 1 LSB and V_{FS} for a 4–bit, 8–bit and 10–bit DAC. $V_{Ref} = 5V$. **(12 Marks)**

b. Determine the DNL and INL for a 3–bit non–ideal DAC with the given output values. Comment on the monotonocity.

Digital code	Analog value
000	0V
001	0.625 V
010	1.5625 V
011	2 V
100	2.5 V
101	3.125 V
110	3.4375 V
111	4.375 V

(08 Marks)

2 a. Draw the transfer curve for a 3–bit ADC with ramp input. Explain what is quantization error. Plot the quantization error graph for an ideal ADC. **(10 Marks)**

b. Explain the mixed signal layout issues. **(10 Marks)**

3 a. Design a 3–bit DAC using binary switch array. Assume $V_{Ref} = 5V$ and power dissipation 5 mW. Find the analog value for the input D = 101. Draw the diagram and the path traced for D = 101. **(08 Marks)**

b. With a neat diagram, explain the working of a cyclic DAC. Find the value of the output voltage at the end of each cycle for N = 4 $V_{Ref} = 5V$ and D = 1101. **(12 Marks)**

4 a. Explain the working of a successive approximation ADC, with a block diagram. For the ADC, give the intermediate values for $V_{Ref} = 8V$, N = 3 and $V_{in} = 3.5V$. **(12 Marks)**

b. Explain the working of a voltage comparator, with the help of a block diagram. **(08 Marks)**

PART - B

5 a. Give the Z domain representation of a two path averager and plot the magnitude and phase response of the digital filter. **(10 Marks)**

b. If the input sinewave to an averager has a peak amplitude of 0.5V and a frequency of 20MHz, determine the peak amplitude of the averager output and the delay through the circuit. **(06 Marks)**

c. Develop an expression for the effective number of bits, in terms of the measured SNR, if the input sinewave has a peak amplitude of 40% of $V_{Ref+} - V_{Ref-}$. **(04 Marks)**

6 a. With the help of a block diagram, explain the accumlate and dump circuit. Plot the general frequency response of an averaging filter. **(10 Marks)**

b. Specify the accuracy required of an 8–bit ADC, if it is to be used to attain 12 bits with INL and DNL of ± 0.5 LSBS $V_{Ref} = 1.5$ V. **(06 Marks)**

c. Discuss the advantages and disadvantages of cascading averaging circuits to increase filter attenuation. **(04 Marks)**

7 a. Explain the concept of interpolation. **(08 Marks)**

b. Explain how MOSFET behaves as a capacitor. Explain floating MOS capacitor. **(08 Marks)**

c. Explain the simple delay element using pass transistors and CMOS inverters. **(04 Marks)**

8 a. Draw the arrangement for a 4 –bit pipelined adder and full adder bit implemented using dynamic logic. **(08 Marks)**

b. Explain the limitation of an inverter at the output of an op-amp, with the help of its transfer curve. How is it overcome? **(06 Marks)**

c. Explain true single phase clocking (TSPC). Using TSPC explain the delay element. **(06 Marks)**

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