**EC/TE/ML403**

**Reg. No.** | | | | | | | | | | |

# Fourth Semester B.E. Degree Examination, July/August 2002

## EC/TE/ML

## Linear IC's and Applications

Time: 3 hrs.] [Max.Marks : 100

**Note:** ***Answer any FIVE full questions.***

**1.** (a) For an emitter coupled differential amplifier obtain an expression for the common mode reflection ratio (CMRR) **(10 Marks)**

(b) Briefly explain the purpose of a constant current source in a differential amplifier. **(5 Marks)**

(c) What is thermal drift? How compensation is obtained in differential amplifier. **(5 Marks)**

**2.** (a) Define the following terms with respect to op.amp. 741C and give their typical values. i) Input offset current ii) Slew rate iii) PSRR iv) Input offset voltage. **(4+2=6 Marks)**

(b) Show how an op amp. can be used as an integrator and a differentiator by obtaining the expression for output voltages. **(6 Marks)**

(c) Design an op.amp. Schmitt trigger circuit with UTP = 2V, LTP = IV, supply voltage = ± 15V, $V_{Sat} = \pm 12V$ **(8 Marks)**

**3.** (a) Draw the circuit diagram of a monostable multivibrator using op.amp and derive an expression for the output pulse width, giving the waveforms. **(12 Marks)**

(b) What are the advantages of active filters over passive filters. **(3 Marks)**

(c) Design an active high pass filter to meet the following specifications.

i) Butterworth response

ii) Cutoff frequency = 4KHz

iii) Decay rate in the stop band = 40dB/decase. **(5 Marks)**

**4.** (a) Show how a 555 IC timer can be used as an astable multivibrator. **(5 Marks)**

(b) Explain the principle of operation of a Sample and Hold Circuit. **(5 Marks)**

(c) With a neat circuit diagram explain the working of a Dual Slope Analog to digital converter mentioning its uses. **(10 Marks)**

**5.** (a) Explain the following terms with reference to digital to analog converter i) Resolution ii) Linearity iii) Accuracy iv) Settling time v) Stability. **(10 Marks)**

(b) A 4 bit digital ramp ADC has an input range of 0 to 7.5 volts. Estimate

i) Resolution

ii) Digital output for an input of 4.25 volts

iii) Conversion time if the clock frequency is IMHz **(7 Marks)**

*Contd.... 2*

**4.** (a) What is the limitation of an ordinary PN junction in rectifier applications ? Explain how an inverting amplifier can be converted to an idial half-wave-rectifier with necessary illustrations. **(8 Marks)**

(b) What is an analog multiplier ? When do you say that the multiplier is a one quadrant multiplier ? Name the applications of a multiplier.
With a block schematic briefly explain a log - antilog multiplier. **(9 Marks)**

(c) Explain the operation of a positive peak detector. **(3 Marks)**

**5.** (a) What are the problems faced by the designer in the design of an analog fitter? How are these problems overcome in an active filter ? **(5 Marks)**

(b) Write the circuit of a narrow band band pass filter using a single OPAMP in the inverting mode. Considering its generalised form, deduce expressions for the following :
i) transfer function for the filter at resonance.
ii) the bandwidth **(8 Marks)**

(c) Design a BPF using a single OPAMP to meet the following characteristics :
Lower cut-off frequency $f_{01} = 3KHz$
Upper cut-off frequency $f_{02} = 3.5KHz$
Gain at resonant frequency is $-5$ **(7 Marks)**

**6.** (a) Briefly explain the basic block diagram of the 555 timer. **(6 Marks)**

(b) Ilustrate the external connections required to design a free-running multi-vibrator using the 555 timer and derive the equation for the frequency of oscillations. **(8 Marks)**

(c) Explain how a PLL can be used to detect an AM signal. **(6 Marks)**

**7.** (a) How are $ADC_s$ broadly classified ? On what principle do they work ?
With a neat schematic and necessary waveforms, explain the operation of the basic voltage - to- frequency ADC circuit. **(12 Marks)**

(b) Discuss briefly the specifications of analog - to - digital converters. **(5 Marks)**

(c) Calculate the values of LSB, MSB, and fullscale output for a 12 - bit DAC, for 0 - 10 volts. **(3 Marks)**

**8.** Explain briefly the following :

a) OPAMP schmitt trigger **(7 Marks)**

b) Sample and Hold circuit **(6 Marks)**

c) $\mu A723$ regulator **(7 Marks)**

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# Fourth Semester B.E. Degree Examination, January/February 2004

## EC/TE/ML

# Linear IC's and Applications

Time: 3 hrs.] [Max.Marks : 100

**Note:** ***Answer any FIVE full questions.***

**1.** (a) Derive an expression for voltage gain, I/p resistance and O/p resistance of single I/p balanced O/p differential amplifier. **(8 Marks)**

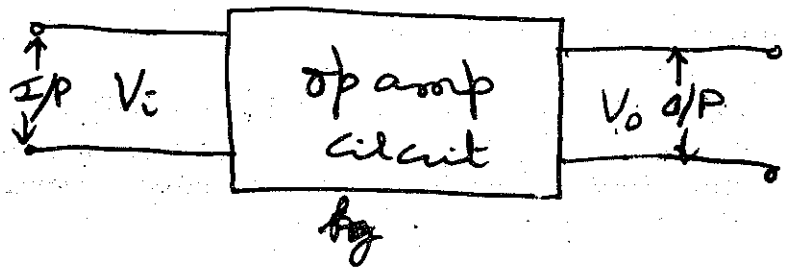
(b) Explain the working of a current mirror circuit. **(6 Marks)**

(c) What is thermal drift? How compensation is obtained in differential amplifier? **(6 Marks)**

**2.** (a) Draw the circuit diagram using op amp to realize the relation

$$V_0 = -[2V_1 + 0.5V_2 + 3V_3]$$ **(4 Marks)**

(b) Draw the circuit diagram to be inserted in the box shown in fig 2(b) which generates the wave form shown in Fig (2 c). Explain its working.

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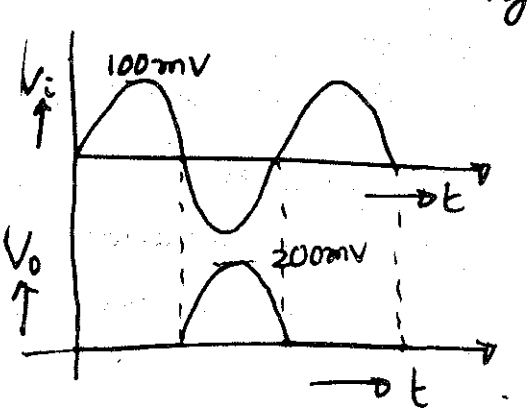



fig 2(b)

fig(2c)

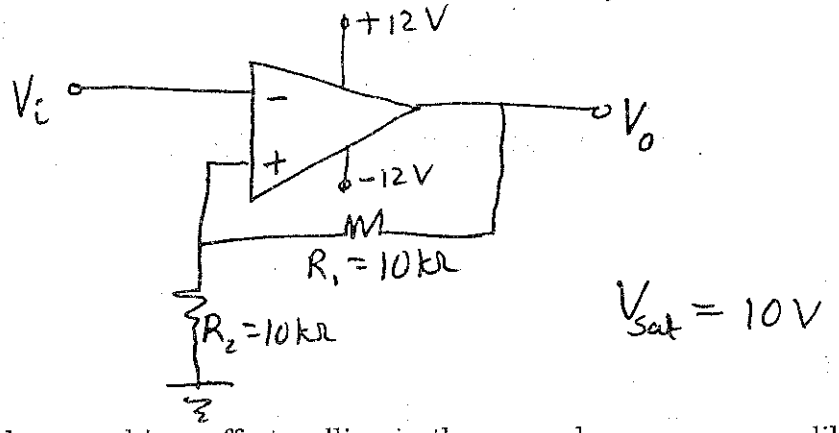
**(6 Marks)**

(c) List the features of instrumentation amplifier. Draw the circuit and derive the expression for o/p voltage. **(10 Marks)**

**3.** (a) Explain the working of free running multivibrator using opamp. Design the same to generate a frequency of 1KHz and derive any expression used. **(12 Marks)**

*Contd.... 2*

(b) For the circuit given below, write the I/p and O/p waveform and plot the transfer characteristic (showing suitable calculation) for $V_i = 20 sin\ wt$.




**(5 Marks)**

(c) How do you achieve offset nulling in the general purpose opamp like $\mu A741$. **(3 Marks)**

**4.** (a) Design an all pass filter to have a phase angle of $+60^0$ if the frequency of $V_{in}$ is 1KHz. Write I/p and O/p waveform. **(8 Marks)**

(b) Explain the working of 1st order wide band pass filter with its frequency response. **(8 Marks)**

(c) The slow rate for a op amp is $0.5V/\mu sec$. At what maximum frequency can you get an undistorted o/p voltage of 1V peak. **(4 Marks)**

**5.** (a) With a neat internal diagram, explain the working of 555 timer as monostable multivibrator. Derive an expression for its pulse width. **(12 Marks)**

(b) With a neat circuit diagram, explain the working of 723 as low voltage regulator. **(8 Marks)**

**6.** (a) Explain the working of 3 bit R-2R ladder type DAC.

For a binary weighted type 4 bit DAC, the O/P is to be 8V for an I/P combination of 0100. Suggest a suitable circuit with component values and reference voltage. For the suggested circuit, estimate the resolution Assume $R_F = 10k\Omega$. **(10 Marks)**

(b) Explain the working of digital ramp ADC. **(6 Marks)**

(c) A 4 bit digital ramp ADC has an I/P range of 0 to 7.5 V. Estimate

i) Resolution

ii) Conversion time if the clock frequency is 1 MHz. **(4 Marks)**

**7.** (a) Explain the various blocks of PLL and its application as frequency multiplier. **(10 Marks)**

(b) Discuss the advantages of switching regulators over series/shunt regulators. Explain its working **(10 Marks)**

**8.** Write short notes on :

i) Frequency and phase compensation techniques in op amp.

ii) V to I converters

iii) 78XX regulators

iv) Performance parameters of data converters. **(20 Marks)**

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# Fourth Semester B.E. Degree Examination, July/August 2004

**EC/TE/ML**

**(Old Scheme)**

## Linear IC's and Applications

Time: 3 hrs.] [Max.Marks : 100

**Note:** ***1. Answer any FIVE full questions.***
***2. All questions carry equal marks***
***3. Missing data if any can be assumed suitably.***

**1.** (a) Write the circuit of dual input balanced output differential amplifier and hence derive the expression for CMRR using h-parameter model. **(12 Marks)**

(b) Design a Dual input balanced output differential amplifier with a constant current bias using diodes to satisfy the following requirements. **(8 Marks)**

i) Differential voltage gain $Ad = 40 \pm 10$

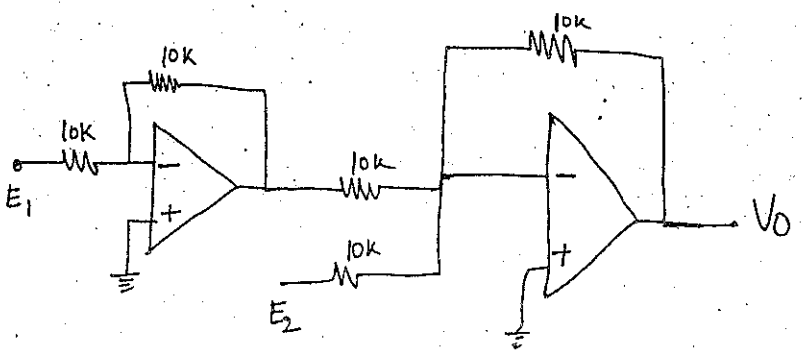
ii) Current supplied by the constant current bias circuit = 4mA

iii) Supply voltages $V_s = \pm 10V$

**2.** (a) Explain the role of a level translator in a differential amplifier with a suitable circuit and write suitable design equations for the same. **(6 Marks)**

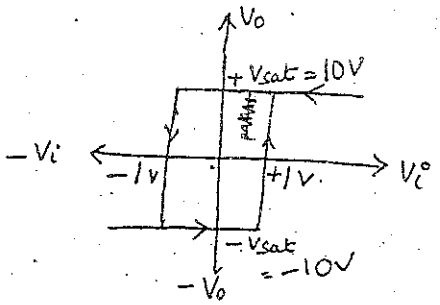
(b) Explain the principle of frequency compensation in an OPAMP. **(8 Marks)**

(c) Calculate $V_o$ shown in the fig below. **(6 Marks)**




**3.** (a) Draw the circuit diagram of an OPAMP monostable multivibrator using OPAMP. With waveforms, derive an expression for output pulse width. **(10 Marks)**

(b) Design a circuit to obtain the following transfer characteristics. **(5 Marks)**




*Contd.... 2*

(c) Explain a non inverting adder with two inputs and derive an expression for output voltage. (Using one OPAMP only). **(5 Marks)**

**4.** (a) Design a lowpass filter to meet the following specifications :

i) Butterworth approximation response

ii) Cutoff frequency = 1 kHz

iii) Falling gain at a rate of 40 dB/dec. **(8 Marks)**

(b) With a suitable diagram explain a basic logamplifier using a diode. How is temperature compensation provided for the above circuit? Hence explain the modified circuit and obtain the expression for output voltage. **(12 Marks)**

**5.** (a) Explain the function of a 555 using its block diagram. How can it be used as an astable multivibrator with duty cycle less than 50%? **(12 Marks)**

(b) Explain a precision type full wave rectifier with a suitable diagram. **(8 Marks)**

**6.** (a) With a neat circuit diagram, explain the working of a dual slope ADC. List its advantages. **(10 Marks)**

(b) Explain the working of a 3 bit flash ADC with a neat diagram. **(6 Marks)**

(c) Suppose that the digital input word for a four bit DAC changes from 0000 to 0110, calculate the DAC's final output voltage. **(4 Marks)**

**7.** (a) Explain how a PLL is used to demodulate FM signal. **(4 Marks)**

(b) Explain the following terms applicable to PLL.

a) Lock in range b) Capture range c) Hold in range. **(6 Marks)**

(c) Design an OPAMP series regulator to meet the following specifications.

$V_i = 18 \pm 3volts$
$V_0 = 9V$
$I_o = 10\ to\ 15mA$
$V_z = 5.6V,\ P_z = 0.5w$ **(10 Marks)**

**8.** Write short notes on any FOUR : **(5×4=20 Marks)**

(a) 3 Pin regulator

(b) Analog multiplier

(c) I to V converter

(d) Switching regulator

e) Peak detector.

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# Fourth Semester B.E. Degree Examination, July/August 2005

## EC/TE/ML

## (Old Scheme)

# Linear Integrated Circuit and Applications

Time: 3 hrs.] [Max.Marks : 100

**Note:** ***Answer any FIVE full questions.***

**1.** (a) What are the advantages of a differential amplifier over d.c. amplifier. **(5 Marks)**

(b) Draw different stages of a typical op-amp and discuss their importance. **(8 Marks)**

(c) Draw the overall frequency response of an op-amp and explain how the stability gets affected when operated in closed loop. **(7 Marks)**

**2.** (a) Define the following applied to one op - amp and give their typical values.

i) Open loop gain

ii) Unity cross-over frequency

iii) Slow rate

iv) Differential input impedance. **(12 Marks)**

(b) An op.amp has to be used in pulse application at $10KHz$. If this op-amp is operated with a power supply voltage of $\pm 10$ volts, calculate the slow rate. **(4 Marks)**

(c) Prove that an non-inverting amplifier can be used as an voltage follower. **(4 Marks)**

**3.** (a) Draw a differentiator using op-amp and indicate the output that will be sean on a C.R.O. if the input given in 2.5 $sin\ wt$. **(5 Marks)**

(b) It is proposed to rectify a sinusoidal signal with an amplitude of 100 microvolts. Suggest a circuit to get positive pulses at the output from negative input swings. Donot use more than one op-amp for a peak output of 5 Volts. **(8 Marks)**

(c) Draw the circuit of an difference amplifier using an OP-amp, that gives an output $V_0 = Arc(V_{i2} - V_{i1})$

Calculate $Arc$ in terms of circuit components. **(7 Marks)**

**4.** (a) Explain the importance of positive feedback in an op-amp comparator, by using transfer characteristic. **(8 Marks)**

(b) Design a monostable that has - $V_{osat}$ as the stable state. The quasi stable state of + $V_{osat}$ exists for 0.1 m sec. Assume $\beta = 0.25$

Draw the waveforms at output, across capacitor and at non- investing terminal and also explain the operation. **(12 Marks)**

Contd.... 2

**5.** (a) What are data converters and where are they used, give typical examples. **(5 Marks)**

(b) Draw the schematic of an 8-bit counter ramp ADC and explain its working. **(10 Marks)**

(c) What will be the converssion time if 1.25 volts is to be converted into binary code using circuit in 5(b) ? What will be the output code ?
Given $V_{inmax} = 5$ Volts and clock frequency $10kHz$. **(5 Marks)**

**6.** (a) It is required to generate symmertical rectangular waves using a timer that has threshold voltage of $\frac{2}{3}V_{cc}$. Design the circuit for a frequency of $5000Hz$. Draw waveforms at different points and explain the operation. **(12 Marks)**

(b) Design an active BP filter having lower cutoff of $2.3KHz$ and upper cutoff of $5KHz$. Draw the bandpass characteristic. Assume the filter is second order. Butterworth with a gain of 3. **(8 Marks)**

**7.** (a) Explain the working of a switching regulator by drawing circuit and waveforms. **(8 Marks)**

(b) IC 723 has to be used to get an output of 2.5volts. Suggest the circuit and design circuit components. Explain the working of designed circuit for a maximum output current of $50mA$. **(7 Marks)**

(c) Explain why switching regulator is prefered over linear regulators. **(5 Marks)**

**8.** Write short notes on :

a) Offset characterstics

b) Analog multipliers

c) Phase locked loop

d) Flash converter **(5×4=20 Marks)**

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# Fourth Semester B.E. Degree Examination, January/February 2006

## EC/TE/ML

## (Old Scheme)

## Linear Integrated Circuits and Applications

Time: 3 hrs.) (Max.Marks : 100

**Note:** ***Answer any FIVE full questions.***

1. **(a)** Give the block diagram approach for the internal structure of an opAmp and explain each block in detail. **(10 Marks)**

   **(b)** Determine voltage gain, input resistance, output resistance, maximum output voltage without clipping for the dual input balanced output differential amplifier as shown in Fig.1.

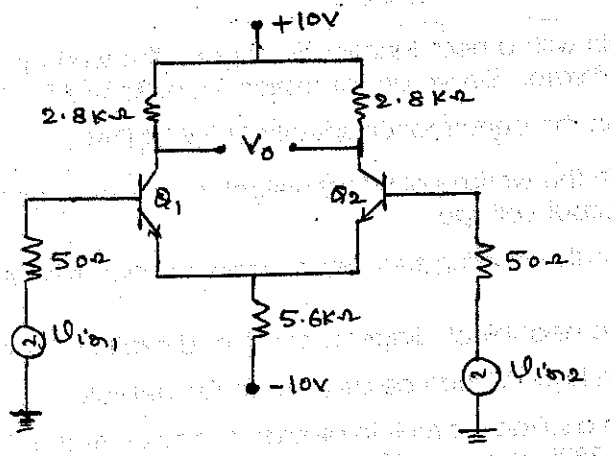


Figure 1.

Also determine output voltage if $v_{in1} = 50mV(p-p)$ and $v_{in2} = 20mV(p-p)$ at 1 kHz. Draw the input and output waveforms. **(10 Marks)**

2. **(a)** What are the ideal electrical characteristics of an opAmp? **(5 Marks)**

   **(b)** Design a zener constant current source as shown in fig.2 according to the following specifications.

   i) Emitter current $I_{E3} = 5mA$,

   ii) IN385 zenerdiode with $V_Z = 4.7V$ and $I_{Zt} = 53mA$

   iii) CA3086 transistor with $\beta_{ac} = \beta_{dc} = 100$ and $V_{BE} = 0.715V$

   iv) supply voltages $V_s = \pm 9V$. **(7 Marks)**

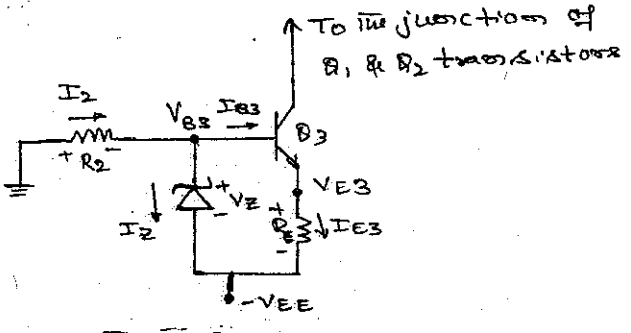


Figure 2.

Contd.... 2

(c) Define the following terms and write their typical values for $\mu$A741 opAmp.
   i) Input bias current
   ii) Input offset voltage
   iii) Slew rate
   iv) CMRR. **(8 Marks)**

**3.** (a) Explain the working of opAmp as a non-inverting amplifier with feedback. Also, derive an expression for voltage gain and input resistance. **(10 Marks)**

(b) Design an opAmp Schmitt trigger circuit with $UTP = 2V$, $LTP = 1V$, supply voltage $= \pm 15V$, $V_{sat} = \pm 13V$. Draw the circuit with designed values. Draw the output waveform when the input is $5sin\omega t$. **(10 Marks)**

**4.** (a) Design a second order butterworth low pass filter with cut-off frequency of 2 kHz. Write the design steps. **(7 Marks)**

(b) What are the advantages of active filters over passive filters? **(3 Marks)**

(c) Explain the astable multivibrator using opAmp and obtain the expression for $T_1$ & $T_2$ and frequency of oscillation. **(10 Marks)**

**5.** (a) Explain with a neat functional diagram the working of 555 timer as a monostable multivibrator. Derive an expression for pulse width. Draw the waveforms. **(12 Marks)**

(b) Explain the performance specifications of DAC. **(8 Marks)**

**6.** (a) Explain the working of Binary weighted network 4-bit DAC. Derive an expression for the output voltage. **(10 Marks)**

(b) Explain the working successive approximation type ADC with a neat diagram. **(10 Marks)**

**7.** (a) Draw a neat block diagram of PLL and explain its working. **(7 Marks)**

(b) Explain how PLL can be used as on FM detector. **(5 Marks)**

(c) Design a suitable circuit to provide a load current of 150 mA to a load of $8\Omega$, $10W$ using 7805 regulator IC. Determine the range of input voltage for satisfactory, operation. **(8 Marks)**

**8.** Write short notes on :

(a) Sample and hold circuits

(b) Thermal drift

(c) V to I converter

(d) Switching regulator. **(5×4=20 Marks)**

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**OLD SCHEME**

# Fourth Semester B.E. Degree Examination, July 2006
## Electronics Communication / Telecommunication
## And Medical Electronics Engineering
## Linear IC's and Applications

Time: 3 hrs.] [Max. Marks:100

**Note :** ***1. Answer any Five full questions.***
***2. Missing data, if any may be assumed suitably***

1 a) Show that for a differential amplifier the output voltage depends on the differential mode gain (Ad) as CMRR tends to infinity. **(04 Marks)**

b) Explain the different stages of an OPAMP with a neat circuit diagram. **(12 Marks)**

c) Discuss the conditions and concept of virtual ground. **(04 Marks)**

2 a) Define the following terms and indicate their typical values for MA74IC OPAMP i) Slew rate, ii) Gain bandwidth product, iii) Input bias current. **(08 Marks)**

b) The following circuit (fig 2.b) has identical transistors with same beta ($\beta$). Show that

$$I_2 = \frac{I_1(\beta)(\beta+1)_1}{(\beta)(\beta+1)+2}$$

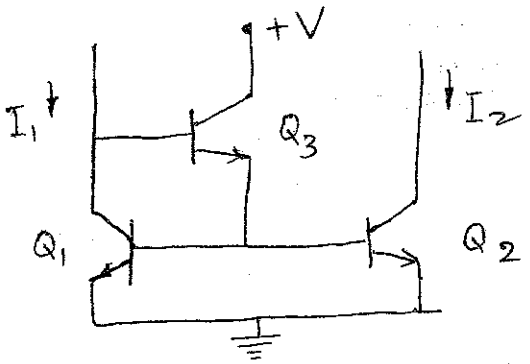


**Fig 2.b**

**(04 Marks)**

c) What is the need of compensation? Explain the different methods of compensation in brief. **(08 Marks)**

3 a) For a Non-Inverting OPAMP with $R_i=\infty$, $R_0=0$, show that $A_{vf}=\frac{A_V(R+R_D)}{(1+A_V)R+R_F}$ where $A_{vf}$: Gain with feed back., $A_V$: Open loop voltage gain. **(08 Marks)**

b) Design an OPAMP circuit to obtain the following output with $A_V=\infty$ and $R_i=\infty$

$$V_0 = -\frac{1}{16}(8V_1 - 4V_2 + V_3)$$ **(06 Marks)**

c) An OPAMP has $R_i=\infty$, $R_0=0$ and $A_V=10^6$. If $R_F$=47k and R=10K, Determine $A_{VF}$, $Z_{if}$ **(06 Marks)**

4 a) Design a practical integrator to integrate the frequency range above 1KHz. Assume $C_F$=0.1MF **(06 Marks)**

b) Draw the circuit diagram of a negative peak detected and explain the function. **(06 Marks)**

c) Design a second order Butter worth Low pass filter with cut off frequency of 200Hz and plot the frequency response of the filter. **(08 Marks)**

5 a) Derive the expression for free running frequency of the 555 Astable Multivibration. Explain with neat circuit diagram. **(10 Marks)**

b) Determine the component values necessary for the 555 timer astable multivibrator having the free running frequency of 900 Hz with 65% duty cycle. Assume timing capacitor C=0.22 $\mu F$ **(10 Marks)**

6 a) Define the following terms : i) Resolution, ii) Linearity, iii) Monotonicity **(06 Marks)**

b) Calculate the values of LSB, MSB, and full scale output and resolution of an 8 bit DA C in the range 0 to 10V. **(04 Marks)**

c) With a neat circuit diagram and wave forms explain the principle of operation of Dual Slope ADC. Also show that the result is independent of RC time constant. **(10 Marks)**

7 a) Explain the principle of operation of a phase locked loop with a neat block diagram. **(06 Marks)**

b) Explain the application of PLL(IC565) for FSK detection with a neat circuit diagram. **(08 Marks)**

c) Draw the functional block diagram of IC 723 regulator and explain how it can be used as a high voltage regulator. **(06 Marks)**

8 Write short notes on any three of the following :

a) Switching regulator

b) Successive approximation ADC

c) Log and antilog amplifiers

d) Schmitt trigger and its applications. **(20 Marks)**

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**OLD SCHEME**

# Fourth Semester B.E. Degree Examination, July 2007
## EC / TE / ML
## Linear IC's and Applications

Time: 3 hrs.] [Max. Marks:100

**Note :** ***1. Answer any FIVE full questions.***
***2. Answers should be to the point.***
***3. Missing data, if any, may be assumed suitably.***

1 a. Write a neat circuit diagram of a dual input balance output difference amplifier. Analyze the circuit using hybrid parameters and hence derive expressions for Ac, Ad and CMRR. **(12 Marks)**

b. Calculate $(V_1 - V_2)$ for the circuit shown: **(04 Marks)**
Assume identical silicon transistors with $V_{BE} = 0.7$ Volts.

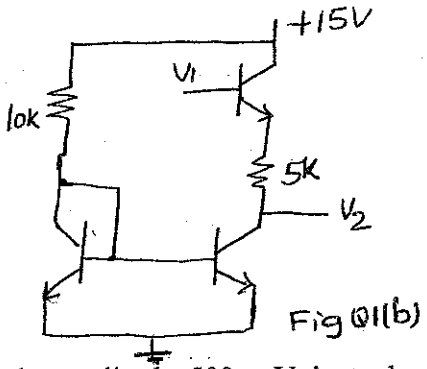

Fig Q1(b)

c. A square wave of peak-peak amplitude 500 mV is to be amplified to peak-peak amplitude of 3 V with a rise time of 4 μsec or less. Can a 741 be used? **(04 Marks)**

2 a. Explain why frequency compensation is necessary for an OPAMP. Discuss in detail different compensation methods. **(12 Marks)**

b. Compute the maximum possible total offset voltage in the circuit shown in fig.2(b) with the following specifications: $V_{io} = 7.5$ mV max, $I_{io} = 50$ nA max, $I_B = 250$ nA max at $25^0$C. i) When $R_{comp}$ is used ii) Without $R_{comp}$. **(08 Marks)**

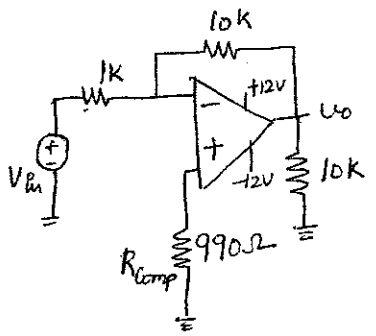

Fig.2(b)

*Contd.... 2*

3 a. With a neat circuit diagram, obtain the expression for output voltage of a bridge amplifier. List some of its uses. **(08 Marks)**

b. Explain a symmetrical square wave generator using an OPAMP and hence derive an expression for its output frequency. **(10 Marks)**

c. List any four OPAMP parameters which are very important in AC applications. **(02 Marks)**

4 a. Write a suitable OPAMP circuit to obtain the transfer characteristics shown below in fig.4(a) and hence explain its working. **(10 Marks)**

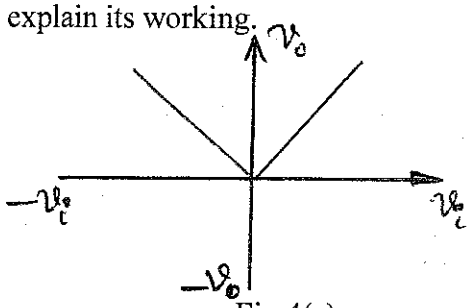


Fig.4(a)

b. Design a 2nd order Butterworth low pass filter having high cutoff frequency of 1 kHz. Draw its frequency response. **(10 Marks)**

5 a. Explain a monostable circuit using 555 timer and derive an expression for output pulse width. **(12 Marks)**

b. Explain the concept of fold back limiting in a 723 regulator IC. **(08 Marks)**

6 a. Explain a 3 bit flash ADC with suitable circuit diagram. **(08 Marks)**

b. Calculate the values of LSB, MSB and full scale output for an 8 bit DAC for 0 to 10 V range. **(05 Marks)**

c. Design a voltage regulator using 723 to get a voltage output of 3 V. **(07 Marks)**

7 a. Explain the application of PLL is frequency translation. **(08 Marks)**

b. List various analog to digital conversion techniques. Which is the faster ADC and why? **(05 Marks)**

c. Explain the principle of switching regulator. **(07 Marks)**

8 Write short notes on the following:

a. Instrumentation amplifier

b. Three pin regulator

c. V-I converter

d. Averaging circuit. **(20 Marks)**

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EC/TE/ML403

# Fourth Semester B.E. Degree Examination, Dec. 07 / Jan. 08
## Linear Integrated Circuits and Applications

Time: 3 hrs. Max. Marks:100

**Note :1.** ***Answer any FIVE full questions.***
**2.** ***Any missing data can suitably be assumed with appropriate comments.***

1 a. Write the circuit of a differential amplifier with constant-current stage in the emitter circuit and explain. Illustrate the input stage of the OPAMP μA 741 with a neat circuit diagram. **(10 Marks)**

b. Discuss the pole-zero cancellation technique as applied to an OPAMP with necessary illustrations. **(06 Marks)**

c. A square wave with negligible rise time and a peak-to-peak voltage of 500 mV must be peak-to-peak amplified to 3 volts with a rise time less than 4 microseconds. Can a μA741 OPAMP be used? **(04 Marks)**

2 a. With neat circuit diagrams for illustration explain the following applications of OPAMP:
i) LOG-Amplifier using two OPAMPS and with a CB transistor in the feed back path.
ii) Ideal Half-wave rectifier. **(14 Marks)**

b. An inverting amplifier configuration is used for summing three input signals of value, $V_1 = 10.5$ V, $V_2 = -2.5$ V, and $V_3 = 4$ V. The resistance in series with the input voltage sources are $R_1 = 5$ kΩ, $R_2 = 10$ kΩ and $R_3 = 8$ kΩ respectively. If the feedback resistance for the scheme is 10 kΩ, assuming that the OPAMP is very poor and has an open loop gain of only 100, determine the magnitude of the output voltage. The input impedance of the OPAMP is 10 kΩ. **(06 Marks)**

3 a. What is an instrumentation amplifier? Where does it find use? List its important features. **(07 Marks)**

b. Write the basic circuit diagram of an instrumentation amplifier that uses three OPAMPS and derive the equation for its output voltage if the input voltages are $V_1$ and $V_2$. **(08 Marks)**

c. Write the circuit of a differential instrumentation amplifier using a transducer bridge and derive an approximate expression for the output voltage. **(05 Marks)**

4 a. What is an active filter? What are its merits and demerits? **(05 Marks)**

b. Draw the scheme of a second order active low-pass filter and deduce the expression for the magnitude of the transfer function in decibels (dB) in terms of the gain, cut-off frequency and damping co-efficient. **(09 Marks)**

c. Design a third order Butterworth low-pass filter with upper cut-off frequency of one kilohertz. **(06 Marks)**

5 a. What is an ADC? How are ADCs broadly classified? Define and give examples for each type. **(06 Marks)**

b. With a neat circuit for illustration, explain the operation of a three-bit Flash-type ADC. What are the factors that limit the conversion time for the above ADC? **(09 Marks)**

c. Discuss briefly the specifications of ADCs. **(05 Marks)**

6 a. What is a phase-locked loop? Write its block schematic. If the PLL is locked-in to the input signal frequency '$f_i$', compute the maximum range of signal frequencies over which the PLL is locked-in interms of the phase-angle-to-voltage transfer co-efficient of the phase detector ($K_\varphi$) and the voltage-to-frequency transfer co-efficient of VCO ($K_v$). **(07 Marks)**

b. With a neat block schematic for illustration explain how a PLL can be used to produce a precise series of frequencies that are derived from a stable crystal controlled oscillator. **(06 Marks)**

c. Illustrate neatly the block diagram and the pin configuration of 565 PLL. List its important features. **(07 Marks)**

7 a. What is a voltage regulator? What do you mean by "fold back current limiting" as applied to a voltage regulator? Explain with necessary illustrations. With usual notations, deduce the equation for short circuit current limit for linear fold back at $V_o$. **(10 Marks)**

b. Design a 15 V, 50 mA supply using the IC regulator μA723 DIP unit. Any relevant information can be assumed with appropriate comments. **(05 Marks)**

c. What is a switching regulator? With a neat block diagram, explain the features of a switching regulator. **(05 Marks)**

8 Explain the following:

a. Schmitt trigger using OPAMP. **(07 Marks)**

b. DAC with R-2R ladder. **(06 Marks)**

c. 555 timer as monostable multivibrator. **(07 Marks)**

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06EC46

# Fourth Semester B.E. Degree Examination, June-July 2009
## Linear ICs and Applications

Time: 3 hrs. Max. Marks:100

**Note:** *1. Answer any FIVE full questions selecting at least TWO from each part.*

### PART – A

1 a. With a neat circuit diagramed explain basic operational amplifier circuit. **(06 Marks)**

b. Explain potential divider bias for an op-amp input, with the necessary design steps. **(06 Marks)**

c. i) With a neat circuit diagram, explain direct-coupled inverting amplifier.
ii) Also, design an inverting amplifier using a 741 op-amp, for which voltage gain is to be 66 and the output voltage amplitude is to be 3V. Given : $I_{B(max)} = 500$ nA. **(08 Marks)**

2 a. Explain the operation of a high input impedance capacitor-coupled voltage follower, with a neat circuit diagram. Obtain the expression for input impedance of the circuit. **(08 Marks)**

b. Briefly discuss the upper cutoff frequency of an op-amp circuit. Show how the cutoff frequency can be set for inverting and noninverting amplifiers. **(06 Marks)**

c. Design a capacitor-coupled inverting amplifier to operate with a + 20V supply. The minimum input signal level is 50mV, the voltage gain is to be 68, the load resistance is 500Ω, and the lower cutoff frequency is to be 200Hz. Use 741 op-amp. **(06 Marks)**

3 a. Define and briefly explain:
i) Loop gain
ii) Loop phase shift
iii) Phase margin
iv) Unity gain bandwidth. **(08 Marks)**

b. With a neat circuit diagram, explain Zin Mod method of frequency compensation. Write the equation for the feedback factor. **(08 Marks)**

c. Calculate the slew rate-limited cutoff frequency for a voltage follower circuit using a 741 op-amp, if the peak of sine wave output is to be 6V. Determine the maximum peak value of the sinusoidal output voltage that will allow the 741-voltage follower. Circuit to operate at the 800 kHz. Unity – gain cutoff frequency. Given : S = 0.5 v/μs. **(04 Marks)**

4 a. With a neat circuit diagram, explain the operation of high input impedance full-wave precision rectifier. Draw the voltage waveforms at various points and write the appropriate equations to show that full-wave rectification is performed. **(12 Marks)**

b. Design an instrumentation amplifier to have an overall voltage gain of 625. The input signal amplitude is 10mV, 741 op-amps are to be used, and the supply is ± 20V. **(08 Marks)**

### PART – B

5 a. With a neat circuit diagram and waveforms, explain the operation of triangular/rectangular wave generator. **(08 Marks)**

b. Explain working of an Wein bridge oscillator with the help of circuit diagram, waveforms and equations. **(06 Marks)**

c. Using a 741 op-amp with a supply of ±15V, design a phase-shift oscillator to have an output frequency of 5.5KHz. Given : Av = 29. **(06 Marks)**

6 a. With a neat circuit diagram and waveforms, explain the operation of inverting Schmitt trigger. **(06 Marks)**

b. Using a 741 op-amp, design a second order high-pass filter to have a cutoff frequency of 15KHz. **(06 Marks)**

c. A capacitor-coupled zero crossing detector is to handle a 2KHz square wave with a peak-to-peak amplitude of 10V. Design a circuit using a 741 op-amp with a ±15V supply. Estimate the minimum op-amp slew rate to give a reasonably undistorted output. Also, calculate the lowest sine wave input frequency that can be applied without the phase shift error exceeding 3°. Given : $V_B = 0.1$ V, $I_{B(max)} = 500$ nA. **(08 Marks)**

7 a. With a neat schematic, explain the salient features of a 723 regulator. **(08 Marks)**

b. Explain the terms line regulation, load regulation and ripple rejection for a dc voltage regulator. **(06 Marks)**

c. What is the principle of switch-mode power supplies? Discuss its advantages and disadvantages. **(06 Marks)**

8 Explain the following with neat diagrams and waveforms:

a. 555 timer as a stable multivibrator

b. 566 voltage controlled oscillator

c. R-2R ladder DAC

d. Dual-slope ADC. **(20 Marks)**

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