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06EC45

Fourth Semester B.E. Degree Examination, May/June 2010
Fundamentals of HDL

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the behavioral and structural description types of HDL programming, with examples and keywords used. **(10 Marks)**

b. Explain the following data types:
i) Physical std_logic and bit_vector in VHDL
ii) Nets, parameters and registers in verilog. **(10 Marks)**

2 a. How do you assign a delay time to the signal assignment statement? Explain the dataflow model of 2×1 multiplexer in VHDL and verilog. **(10 Marks)**

b. Explain the use of data type vectors with dataflow description of 2×2 unsigned combinational array multiplier in VHDL and verilog. **(10 Marks)**

3 a. Differentiate between signal and variable assignment statement in VHDL. Write VHDL programs for behavioral description of D-latch using signal assignment and variable assignment. **(10 Marks)**

b. Explain the formats of for-loop and while-loop statements in VHDL and verilog. **(06 Marks)**

c. Write verilog description for a 4-bit priority encoder. **(04 Marks)**

4 a. Explain the binding in the following, with example:
i) Between entity and component in VHDL
ii) Between two modules in verilog. **(10 Marks)**

b. Write the HDL programs for N+1 bit magnitude comparator using
i) generate and generic in VHDL ii) generate and parameter in verilog. **(10 Marks)**

PART – B

5 a. Explain the use of procedure (in VHDL) and task (in verilog) with description of full adder, using half adders. **(10 Marks)**

b. Explain the file declaration and built in procedures for file handling in VHDL. **(10 Marks)**

6 a. How to attach a package to the VHDL module? Explain with an example. **(08 Marks)**

b. What is the need of mixed type descriptions? Write description of 16×8 SRAM in VHDL and verilog. **(12 Marks)**

7 a. How to imvoke a VHDL entity from a verilog module. Explain with an example. **(10 Marks)**

b. Write a HDL program for mixed language descriptions of a JK-flip-flop with a clear input. **(10 Marks)**

8 a. Write a flow diagram of synthesis. Explain its steps. **(08 Marks)**

b. Write VHDL code for signal assignment statement y = 2 * x + 3. Show the synthesized logic symbol and gate level diagram. Write structural code in verilog using the gate level diagram. **(12 Marks)**

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