

**Third Semester B.E. Degree Examination, Dec. 07 / Jan. 08**  
**Logic design**

Time: 3 hrs.

Max. Marks:100

**Note :** 1. Answer any FIVE full questions.  
 2. Assume missing data if any suitably.

- a. Two motors  $M_2$  and  $M_1$  are controlled by three sensors  $S_3$ ,  $S_2$  and  $S_1$ . One motor  $M_2$  is to run any time all three sensors are on. The other motor is to run whenever sensors  $S_2$  or  $S_1$  but not both are on and  $S_3$  is off. For all sensor combinations where  $M_1$  is on,  $M_2$  is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation. (06 Marks)
- b. Simplify using Karnaugh map. Write the Boolean equation and realize using NAND gates.  $D = f(w, x, y, z) = \Sigma(0,2,4,6,8) + \Sigma d(10,11,12,13,14,15)$ . (06 Marks)
- c. Simplify  $P = f(a, b, c) = \Sigma(0,1,4,5,7)$  using two variable Karnaugh map. Write the Boolean equation and realize using logic gates. (08 Marks)
- a. Simplify using Karnaugh map  $L = f(a, b, c, d) = \pi(2,3,4,6,7,10,11,12)$  (06 Marks)
- b. Simplify using Quine Mc Cluskey tabulation algorithm-  
 $V = f(a, b, c, d) = \Sigma(2,3,4,5,13,15) + \Sigma d(8,9,10,11)$  (14 Marks)
- a. Design a combinational circuit that will multiply two two-bit binary values. (08 Marks)
- b. Design a 4 to 16 decoder using two 3 to 8 decoder (74LS138). (06 Marks)
- c. Design a keypad interface to a digital system using ten line BCD encoder (74LS147). (06 Marks)
- a. Design a binary full subtractor using minimum number of gates. (06 Marks)
- b. Explain the terms  
 i) Ripple – carry propagation  
 ii) Propagation delay  
 iii) Look- ahead carry  
 iv) Iterative design. (04 Marks)
- c. Realize  $F = f(x, y, z) = \Sigma(1,2,4,5,7)$  using 8 – to – 1 multiplexer (74LS151). (04 Marks)
- d. Design a two bit binary magnitude comparator. (06 Marks)
- a. Explain with timing diagram the working of a S. R latch as a switch debouncer. (06 Marks)
- b. Explain the working of a Master – slave JK Flip-Flop with functional table and timing diagram. Show how race around condition of master-slave SR Flip-Flop is over come. (08 Marks)
- c. What is the significance of edge triggering? Explain the working of edge triggered D-flip-flop and T-flip-flop with their functional table. (06 Marks)
- a. Obtain the characteristic equation for a SR flip-flop (04 Marks)
- b. With a neat circuit diagram, explain the working of a universal shift register. (08 Marks)
- c. Design a synchronous Mod-6 counter using clocked J K flip-flop. (08 Marks)

- 7 a. Explain mealy and Moore sequential circuit models. (04 Marks)
- b. For the state machine  $M_1$  shown in Fig. Q 7(b), obtain
- State table
  - Transition table
  - Exaltation table for T flip-flop
  - Logic circuit for T exaltation realization.

(16 Marks)

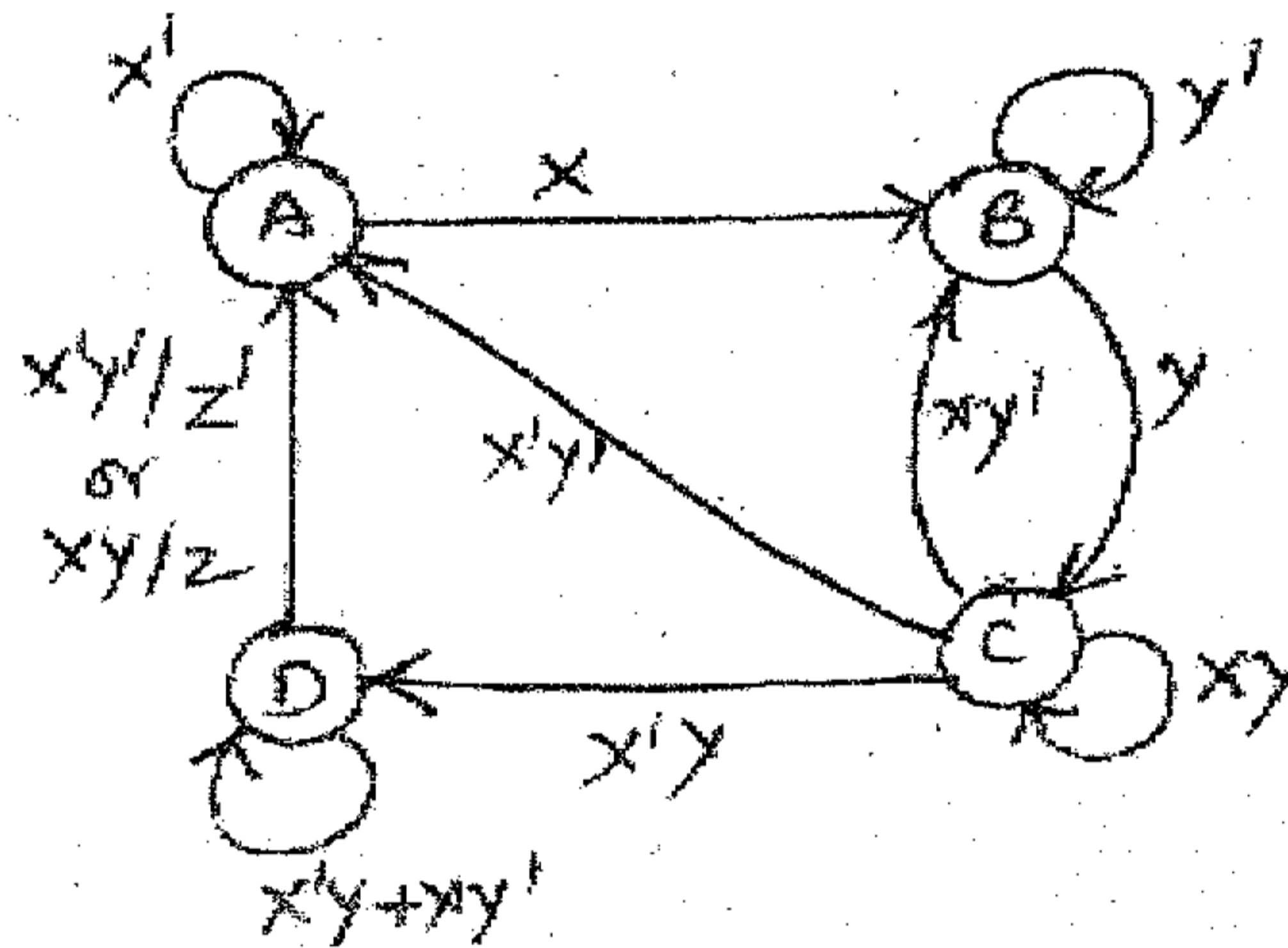


Fig. Q 7(b)

- 8 a. Construct a mealy state diagram that will detect a serial sequence of 10110. When the input pattern has been detected, cause an output Z to be asserted high. (08 Marks)
- b. Design a cyclic modulo-8 synchronous counter using J-K flip-flop that will count the number of occurrences of an input; that is, the number of times it is a 1. The input variable X must be coincident with the clock to be counted. The counter is to count in binary. (12 Marks)

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