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06CS46

Fourth Semester B.E. Degree Examination, May/June 2010
Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. PC contains the address of the instruction stored in main memory of the computer. The instruction is "MOVE (R3), R2". List the steps needed to execute the machine instruction MOVE (R3), R2. **(08 Marks)**

b. Explain with examples, all the generic addressing modes, with assembler syntax. **(12 Marks)**

2 a. Convert the following pairs of signed decimal numbers to 5 bit 2's. Complement the numbers and add them. State whether overflow occurs or not.
i) -14 and 11 ii) -10 and -13 iii) -3 and -8. **(06 Marks)**

b. What is word alignment of a machine (microprocessor based system)? Explain. What are the consecutive addresses of aligned words for 16, 32 and 64 bit word lengths of machines? Give two consecutive addresses for each case. **(05 Marks)**

c. Bring out the five key differences between subroutine and interrupt service routine. **(05 Marks)**

d. What is the function of an assembler directive? Give two examples of assembler directives used for the reservation of memory locations for variables. State their functions. **(04 Marks)**

3 a. Define and explain briefly the following:
i) interrupt.
ii) vectored interrupt.
iii) interrupt nesting.
iv) an exception and give two examples. **(13 Marks)**

b. Explain in brief, with the help of a diagram, the working of daisy chain with multiple priority levels and multiple devices in each level. **(07 Marks)**

4 a. In a computer system, PCI bus is used to connect devices to the processor (system bus) bus. Consider a bus transaction in which the processor reads four 32-bit words from the memory. Explain the read operation on the PCI bus between memory and processor. Give signal and timing diagram. **(12 Marks)**

b. Draw the block diagram of universal bus (USB) structure connected to the host computer. Briefly explain all fields of packets that are used for communication between a host and a device connected to an USB port. **(08 Marks)**

PART – B

5 a. Define and explain the following :
i) Memory access time ii) Memory cycle time
iii) Random access memory (RAM) iv) Static memories. **(04 Marks)**

b. Differentiate the static RAM (SRAM) and dynamic RAM (DRAM) giving four key differences. State the primary usage of SRAM and DRAM in contemporary computer systems. **(04 Marks)**

c. Define memory latency and bandwidth in case of burst operation that is used for transferring a block of data to or from synchronous DRAM memory unit. **(05 Marks)**

d. Draw a neat block diagram of memory hierarchy in a contemporary computer system. Also indicate relative variation of size, speed and cost per bit, in the hierarchy. **(07 Marks)**

6 a. Explain a simple method of translating virtual address of a program into physical address, with the help of a diagram. **(08 Marks)**

b. Explain structural organization of moving head magnetic hard disk, with multiple surfaces for storage of data. Explain how moving head assembly works for reading data. **(06 Marks)**

c. Answer the following with respect to the magnetic disk, the secondary storage device:
i) seek time
ii) latency
iii) access time **(06 Marks)**

7 a. In carry – look ahead addition, explain generate G_i and propagate P_i functions for stage i with the help of Boolean expression for G_i and P_i . **(04 Marks)**

b. Perform signed multiplication of numbers -12 and -11 using both multiplication algorithm. Represent the numbers in 5-bits including sign bit. Give booth multiplier recoding table that is used in the above multiplication. **(08 Marks)**

c. Perform division of number 8 by 3 (8 ÷ 3) using non-restoring division algorithm. **(08 Marks)**

8 a. Draw the block diagram of the three-bus organization of data path, which providess multiple internal paths to enable several transfers to take place in parallel. Label the registers and functional components of the processor and their connection to the respective bus of data path. **(16 Marks)**

b. Draw a block diagram of a complete processor and identify the units. **(04 Marks)**

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