Third Semester B.E. Degree Examination, May/June 2010
Logic Design

Time: 3 hrs. Max. Marks:100

Note: *Answer any FIVE full questions, selecting at least TWO questions from each part.*

PART – A

1 a. Simplify the given Boolean function by using K-map method and express it in SOP form. Realise logic circuit by using NAND gates only.

$$f(A, B, C, D) = \sum (m(7, 9, 10, 11, 12, 13, 14, 15))$$ (06 Marks)

   b. Simplify following Boolean function by using K-map method in POS form:

$$f(A, B, C, D) = \sum m(0, 1, 2, 3, 4, 5, 7)$$ (06 Marks)

   c. Find prime implicants for the Boolean expression by using Quine McClusky method.

$$f(A, B, C, D) = \sum (1, 3, 6, 7, 8, 9, 10, 12, 14, 15) + d(11, 13)$$ (08 Marks)

2 a. Define decoder. Draw logic diagram of 3:8 decoder with enable input. (06 Marks)
   b. Implement the given Boolean function by using 8:1 multiplexer.

$$f(A, B, C, D) = \sum (0, 1, 3, 5, 7, 11, 12, 13, 14)$$ (06 Marks)

   c. With a neat diagram, explain the decimal to BCD encoder. (08 Marks)

3 a. What are the three different models for writing a module body in verilog HDL? Give example for any one model. (06 Marks)
   b. With truth table and a neat logic diagram, explain full adder implementation. (06 Marks)
   c. Explain how IC 7483 can be used as 4 bit adder/subtractor. (08 Marks)

4 a. With transfer characteristic, explain how Schmitt trigger converts a random waveform into a rectangular waveform. (06 Marks)
   b. Explain basic S.R flip-flop by using NOR gate. What is the drawback of S-R flip-flop? How J-K flip-flop is obtained from S-R flip-flop? (08 Marks)
   c. Find out characteristic equations of J-K flip-flop and D flip-flop. (06 Marks)

PART – B

5 a. Explain any two types of shift register with waveforms. How Johnson counter is obtained from shift register? (10 Marks)
   b. Design Mod-6 synchronous counter by using J-K flip-flop. Give excitation table of J-K flip-flop, state diagram and state transition table. (10 Marks)

6 a. Differentiate between Moore and Mealy model of synchronous sequential circuit. (04 Marks)
   b. Reduce the state transition diagram of Mealy model by row elimination method and implication table method. (16 Marks)
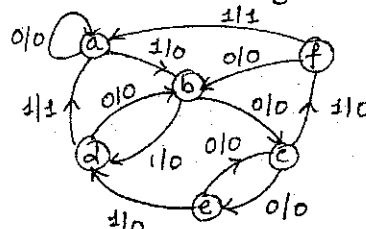
State transition diagram.

Fig. Q6 (b)

7 a. Explain with neat diagram, R-2R ladder type 4 bit D to A converter. Find out analog output if input is 1100 and '1'= +5 volts. For 10 bit DAC if full scale output is 10.24 volts, what is resolution? **(10 Marks)**

   b. Explain with a neat diagram, successive approximation type DAC. **(10 Marks)**

8 a. With a neat circuit diagram, explain the operation of a two input TTL NAND gate with tolem pole output. **(08 Marks)**

   b. Explain with a neat diagram, CMOS inverter. **(06 Marks)**

   c. Explain CMOS characteristics. **(06 Marks)**

* * * * *