

Sixth Semester B.E. Degree Examination, June/July 2013
Microelectronic Circuits

Time: 3 hrs.

Max. Marks:100

Note: Answer FIVE full questions, selecting at least THREE from Part A and TWO from Part B.

PART - A

- 1 a. Derive the equation for finite output resistance of a MOSFET. (08 Marks)
- b. For the CS-amplifier shown in Fig.Q.1(b), find R_{in} , A_{v_o} , R_{out} and G_v with r_o taken into account. If V_{sig} is a 0.4V (P-P) what output signal results? Assume $R_{sig} = 10K\Omega$, $R_L = 15K\Omega$, $g_m = 1 \text{ mA/v}$ and $r_o = 150K\Omega$. (08 Marks)

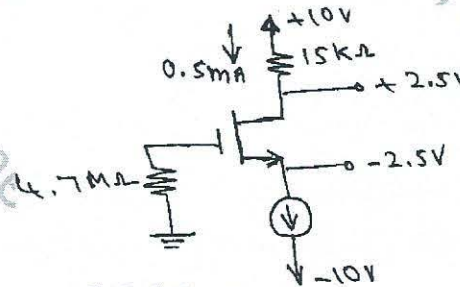


Fig.Q.1(b)

- c. What is threshold voltage and mention its range? (04 Marks)
- 2 a. Draw the development of the T-equivalent circuit model for the MOSFET. (05 Marks)
- b. Derive the voltage gain and overall voltage equations of a source follower using MOSFET. (08 Marks)
- c. Design the circuit shown in Fig.Q.2(c) so that the transistor operates at $I_D = 0.4 \text{ mA}$ and $V_D = 0.5V$. The NMOS transistor has $V_t = 0.7V$, $\mu_n C_{ox} = 100 \mu \text{ A/V}^2$, $L = 1\mu\text{m}$ and $W = 32 \mu\text{m}$. Neglect the channel length modulation effect. (07 Marks)

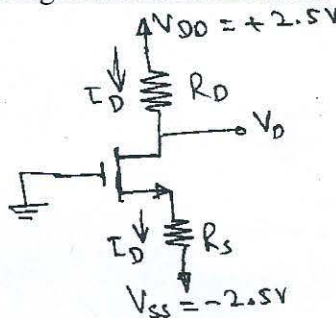


Fig.Q.2(c)

- 3 a. What is MOSFET scaling? Mention the benefits of scaling. (06 Marks)
- b. Draw the MOSFET constant current source circuit and explain it. (06 Marks)
- c. Explain the operation of a MOS current steering circuit and mention its advantage. (08 Marks)
- 4 a. What is cascade amplifier? Explain the operation of a MOS cascade amplifier. (07 Marks)
- b. Draw the high frequency-equivalent circuit model of the MOSFET common source amplifier and explain the significance of each element. (07 Marks)
- c. Draw the three different transistor pairings and explain each configuration. (06 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
 2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

- 5 a. Explain the operation of MOS differential pair with a differential input voltage. (07 Marks)
 b. Draw the circuit diagram of a active-loaded MOS differential pair and explain it. (08 Marks)
 c. What are the features of two-stage CMOS op-amp configuration? (05 Marks)

PART – B

- 6 a. Explain the effect of feedback on the amplifier poles. (06 Marks)
 b. What are the properties of negative feedbacks? Explain in detail. (08 Marks)
 c. Draw the ideal structure for the series-series feedback amplifier and explain it. (06 Marks)
- 7 a. Explain how to minimize the temperature effect in a logarithmic amplifier. (08 Marks)
 b. Draw the sample and hold circuit using op-amp and explain it. (07 Marks)
 c. Design a non-inverting op-amp with a gain of 2. At the maximum output voltage of 10V and the current in the voltage divider is to be $10\mu\text{A}$. (05 Marks)
- 8 a. What are the reasons for choosing CMOS over bipolar technology in digital applications? (04 Marks)
 b. Explain the dynamic operation of a CMOS inverter. (10 Marks)
 c. Implement $F = \overline{AB + CD}$ using the AOI gate. (06 Marks)
