USN | 1 | M | V | 1 | 0 | E | C | 1 | 0 | 7 | | 10ES33

Third Semester B.E. Degree Examination, December 2011
Logic Design

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Expand $f_1 = a + bc + a\bar{c}d$ into minterms and $f_2 = a(b + c)(a + c + \bar{d})$ into maxterms. **(06 Marks)**

b. Simplify $f(a, b, c, d) = \sum m(1, 2, 4, 11, 13, 14, 15) + dc(0, 5, 7, 8, 10)$ using Karnaugh map technique. **(05 Marks)**

c. Obtain a minimal SOP expression for the function $f(a, b, c, d, e) = \sum m(3, 7, 11, 12, 13, 14, 15, 16, 18) + dc(24, 25, 26, 27, 28, 29, 30, 31)$ using Karnaugh map method. **(05 Marks)**

d. Explain canonical form of Boolean equations with an example. **(04 Marks)**

2 a. Minimize $f(a, b, c, d) = \pi(0, 6, 7, 8, 9, 13) + \pi dc(5, 15)$ using quine Mc cluskey method. **(12 Marks)**

b. Simplify $f(a, b, c, d) = \sum m(2, 3, 4, 5, 13, 15) + dc(8, 9, 10, 11)$ taking least significant bit as map entered variable. **(08 Marks)**

3 a. Design and implement a 4 bit look ahead carry adder. **(14 Marks)**

b. Implement 16:1 multiplexer using 4:1 multiplexers. **(06 Marks)**

4 a. Design and implement a 2 BIT digital comparator. **(09 Marks)**

b. Implement a full subtractor using 3 – 8 line decoder with the decoder having high outputs and active low enable thermal. **(05 Marks)**

c. Implement the Boolean function $f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 9, 10, 15)$ using multiplexer with a, b connected to select lines s_1, s_0. **(06 Marks)**

PART – B

5 a. Give the NAND – NAND implementation of a gated SR latch with preset and clear facilities, such that when preset = 0, the output should be 1 while clear = 0, the output be 0. Give the truth table clearly indicating gate, clear, preset and input signals and the corresponding outputs. **(07 Marks)**

b. Explain the working of a pulse triggered JK master slave flip flop with a truth table. **(06 Marks)**

c. Explain the functioning of positive edge triggered D – flip flop. **(07 Marks)**

6 a. Explain 4 bit universal shift register using negative edge triggered D – flip flops. **(08 Marks)**

b. Give the circuit of a 4 bit JOHNSON counter using negative edge triggered D flip flops. Draw the timing waveforms with respect to clock starting with an initial state of $Q_3Q_2Q_1Q_0 = 0000$. What is the modulus of this counter? **(08 Marks)**

c. What is meant by triggering of flip flops? Name the different triggering methods. **(04 Marks)**

7 a. Compare synchronous and ripple counters. **(03 Marks)**

b. Draw the circuit of a 3 BIT, asynchronous, down counter using negative edge triggered JK flip flops and draw the timing waveforms. **(05 Marks)**

c. Design and implement a synchronous counter to count the sequence 0 – 3 – 2 – 5 – 1 – 0 using negative edge triggered JK flip flops. **(12 Marks)**

8 a. Explain Mealy and Moore machine models. **(06 Marks)**

b. Construct the excitation table, transition table, state table and state diagram for the Moore circuit shown in Fig.Q.8(b). **(14 Marks)**

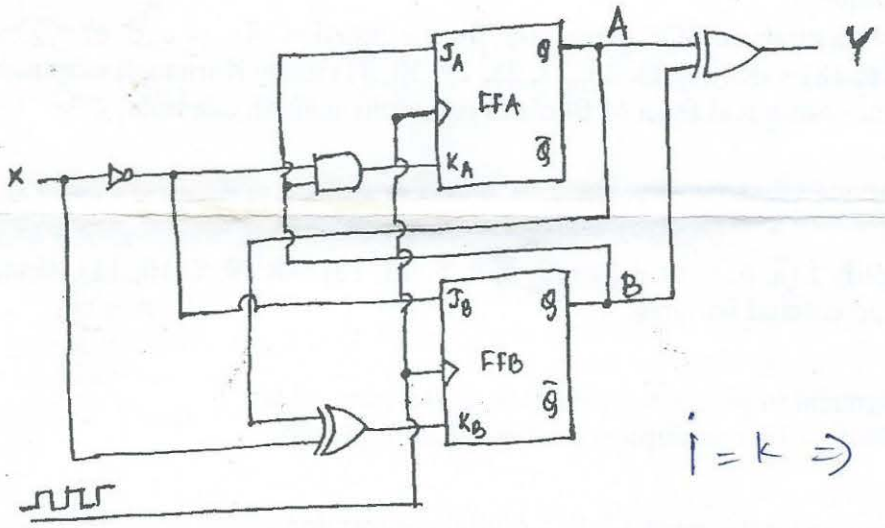

Fig.Q.8(b)

$$C_i = \frac{1}{16} \sum_{n=5}^{20} b_T(n)\, v(n+i)$$

$$v(n) = \sum_{k=0}^{5} b_T(n-k)\, f_k \qquad *****$$

$$v(n+i) = \sum_{k=0}^{5} b_T(n-k+i)\, f_k$$

$$C_i = \frac{1}{16} \sum_{n=5}^{20} b_T(n) \sum_{k=0}^{5} b_T(n+i-k)\, f_k$$

$$C_i = \frac{1}{16} \sum_{k=0}^{5} f_k \sum_{n=5}^{20} b_T(n)\, b_T(n+i-k)$$

$i = k \Rightarrow$

shifts in fixed seq = channel coeff index

f_0
f_1 1 2 3 4
f_2
f_3 2 3 4 1
f_4 5 6 3 4 1 2
f_5 2 4 1 3 4 2

C_i = corr res for i shifts in fixed seq

Let $i = k$ where