EC835

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NEW SCHEME

Eighth Semester B.E. Degree Examination, May 2007
Electronics and Communication Engineering
Embedded System Design

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Explain the various metrics that need to be optimized while designing an embedded system. **(08 Marks)**

b. Explain the three main processor technologies that can be used with embedded system. Also highlight the benefits of each. **(06 Marks)**

c. Explain how the top-down design process improves the productivity. **(06 Marks)**

2 a. Explain the various steps involved in designing a custom single-purpose processor. **(06 Marks)**

b. Explain the concept of 'data path' in the embedded systems. **(04 Marks)**

c. Design a single-purpose processor that outputs Fibonacci numbers upto n. Start with a function computing the desired result, translate it into a state diagram and sketch a probable datapath. **(10 Marks)**

3 a. Explain the various events that take place when a processor executes an instruction. Explain how does pipelining improves the execution speed. **(08 Marks)**

b. Explain the various addressing modes that are commonly used by processors. **(04 Marks)**

c. Explain the steps involved in designing a general-purpose processor. **(08 Marks)**

4 a. Explain how UART is used for communication highlighting the advantages of UART. **(06 Marks)**

b. Schematically explain how a PWM helps in controlling the speed of DC motor. **(06 Marks)**

c. Highlight the advantages of using data in digital form over its analog form. Explain the working of successive approximation type of analog to digital converter. **(08 Marks)**

5 a. Explain the various types of RAM highlight the features of each. **(06 Marks)**

b. What is cache memory? Explain its need and how it helps in improving the execution speed. **(06 Marks)**

c. With a neat diagram explain the advanced RAM architecture. Also explain how this is extended to improve the performance through synchronous DRAM. **(08 Marks)**

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6 a. What is multi-level bus architecture? Explain its need and also the reasons to improve the processor performance by this architecture. **(06 Marks)**

b. Explain the reasons that make the serial communication more preferred than the parallel communication systems. **(06 Marks)**

c. Explain how I^2C bus structure in peripherals to communicate with the processor. **(08 Marks)**

7 a. Explain the need for interrupts in processing systems. Also explain the various events that take place when a processor is interrupted. **(06 Marks)**

b. Explain the problems associated with interrupts that deals with the shared-data. Also suggest solutions to solve these problems. **(08 Marks)**

c. What is interrupt latency? Explain the factors affecting it. **(06 Marks)**

8 a. Explain the reasons why the systems with the conventional operating system fail to respond to the real time problems. Also explain how these are taken care in RTOS. **(06 Marks)**

b. Explain the concept of semaphores. How these help us in solving the shared – data problem in embedded systems? **(08 Marks)**

c. Differentiate between hard and soft RTOS highlighting the advantages and disadvantages of each. **(06 Marks)**

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EC835

Eighth Semester B.E. Degree Examination, Dec. 07 / Jan. 08

Embedded System Design

me: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

a. Define an embedded system. Briefly explain its 3 characteristics that distinguish such systems from other systems. Write the block diagram of a digital camera. **(06 Marks)**

b. Derive the formula for percentage revenue loss. If the lifetime of a product is 72 weeks, delay in time to market is 12 weeks, determine the percentage revenue loss. If NRE cost is $100000, total number of units is 2000 and unit cost is $250, determine the per product cost. **(08 Marks)**

c. Differentiate between SPP and ASIP. **(06 Marks)**

a. Explain the top down design process used in design technology. **(06 Marks)**

b. Write and compare any two algorithms for GCD computation. **(08 Marks)**

c. Show how FSDM can be optimized for GCD computation for any one of the algorithms for GCD computation. **(06 Marks)**

a. Define the following:
i) Linker ii) Cross compiler iii) Latency
iv) Datapath v) Device driver vi) Device programmer. **(06 Marks)**

b. Describe the working of a PWM unit with timing diagrams. How it can be used for speed control of DC motor. **(08 Marks)**

c. Explain pipelining technique. Determine the speedup of a pipelined processor over a non-pipelined processor if 4000 instructions are executed in an 8 stage pipelined processor whose clock frequency is 20 MHz. **(06 Marks)**

a. Given a 16 bit timer with 20 MHz,
i) Determine its range and resolution
ii) Calculate the terminal count value needed to measure 1.5 msec interval
iii) If a prescaler is added, what is the minimum division needed to measure an interval of 50 msec. Determine its range and resolution, if the division value is a power of 2. **(06 Marks)**

b. Determine the resolution of an 8 bit ADC with an analog input voltage range of 0 to 5 V. Determine the digital encoding for 3.5 Volts using a formula and trace the steps using successive approximation technique. Write successive approximation technique. Write the steps for this technique in the form of a table, with necessary columns / informations. **(08 Marks)**

c. Write two differences between:
i) ROM and R/w M
ii) PSRAM and NVRAM
iii) SRAM and DRAM. **(06 Marks)**

5 a. Write block schematics to increase the number of bits in a memory and also to increase the number of memory locations. Compare 2 k × 8 ROMs into a 4 k × 16 ROM. **(06 Marks)**

b. Describe fully associative cache mapping technique. In a memory hierarchy design consisting of cache and main memory, the cache miss rate is 15%, cost of memory access is 20 cycles and cost of cache access is 20 cycles and cost of cache access is 2 cycles. Determine the average cost of access. **(08 Marks)**

c. Explain the features of CAN bus and IEEE 802.11 protocols. **(06 Marks)**

6 a. Describe shared data problem with an example and algorithm. **(06 Marks)**

b. Define interrupt latency. What are the 4 factors/parameters involved in it? Let the high, medium and low priority processes require an execution time of 150 μsec, 250 μsec and 350 μsec respectively. If the interrupts are disabled for 200 μsec and the deadline for the low priority process is 850 μsec, determine its worst case interrupt latency. Can it meet the deadline, if the other two interrupts occur? Illustrate with a timing diagram. **(08 Marks)**

c. Describe round robin architecture with an example. **(06 Marks)**

7 a. What are semaphores and critical sections? Explain P and V algorithms for locking and unlocking a resource for binary semaphore variable. **(06 Marks)**

b. Describe the function of a scheduler with a state transition diagram and the relationship between task and data. **(08 Marks)**

c. Explain the use of message queues with an example or algorithm. **(06 Marks)**

8 a. Explain "encapsulating semaphores" with an algorithm. **(06 Marks)**

b. Describe the two rules that an RTOS environment must follow for interrupt routines. **(08 Marks)**

c. Explain how memory space can be saved in hard real time scheduling with an example. **(06 Marks)**

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EC835

Eighth Semester B.E. Degree Examination, May/June 08
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Differentiate between the following
   i) Single purpose and general purpose processors.
   ii) Full custom IC and PLD technologies **(08 Marks)**

b. Explain the following terms
   i) Characteristics of an embedded system
   ii) Ideal top – down design process. **(06 Marks)**

c. Define time – to – market and NRE cost metrics. The lifetime of a product is 64 weeks. If the product is delayed by 7 weeks, determine the percentage revenue loss. Determine the per – product cost, if the NRE cost is Rs 4,00,000 and unit cost is Rs 8000 and the company produces 5000 units of that product. **(06 Marks)**

2 a. Write s simple algorithm for finding the GCD of two integer numbers. Write the FSMD for this algorithm and explain how it can be optimized and write the optimized FSMD and its advantages. **(14 Marks)**

b. Explain the following 3 addressing modes with an example from any processor.
   i) Register indirect
   ii) Relative addressing
   iii) Direct **(06 Marks)**

3 a. Explain the following terms
   i) Superscalar architecture
   ii) Linker
   iii) Dhrystone Benchmark
   iv) Cross compiler **(08 Marks)**

b. Differentiate between
   i) Harvard and Princeton architectures
   ii) Microcontrollers and DSPs. **(06 Marks)**

c. Explain pipelining. If 6000 instructions are to be executed using a 4 stage pipelined processor at a clock frequency of 12 MHz, determine the speedup of the pipelined processor when compared to a non – pipelined processor. **(06 Marks)**

4 a. Describe the working of PWM with necessary diagrams and explain how it can be used in the speed control of DC motor. **(08 Marks)**

b. What is a WDT and what is its use? A 16 bit timer operates at a clock frequency of 20 MHz. Determine the resolution and range of this timer. If a ÷ 4 – prescaler is also used, what is the range and resolution of this design? **(06 Marks)**

c. The analog input range for an 8 bit ADC is from –2.5 V to + 7.5 V. Determine the resolution of ADC and digital output in hexadecimal when the input voltage is 1.2 V. Trace successive approximation steps and show the binary output of the ADC. **(06 Marks)**

5 a. Compare the following
   i) SRAM and DRAM
   ii) Direct mapped and fully associative cache memory designs. (08 Mar

b. Explain the following terms in brief
   i) Flash memory
   ii) NVRAM
   iii) IrDA (06 Mar

c. Compose 1k × 8 ROMs for the design of a 2 k × 16ROM. Write a block diagram showi the connections and the memory map. Determine the average memory access time, if t cache miss ratio is 0.2, cache access requires 2 cycles and main memory access requires cycles when the clock frequency is 20 MHz. (06 Mar

6 a. Explain shared data problem with an example show how interrupt facility can be used solving this problem. (08 Mar

b. Compare i) CAN Bus and PCI Bus ii) Serial and Parallel communication. (06 Mar

c. Consider three processes with high, medium and low priorities respectively. The executi time values of these three processes be 100μ sec, 200μ sec and 300μ sec respectively. T minimum interrupts latency of the system be 150μ sec. Let the deadline of the low prior process be 600μ sec. Is it possible for the low priority process to execute before t deadline if the other two interrupts also occur or only medium priority process interru it? Determine the worst case Interrupt latency values for both the cases. (06 Mar

7 a. Describe RR with interrupts with an algorithm. Mention a practical application for t same. (08 Marl

b. Explain RTOS architecture with an algorithm. (06 Marl

c. Compare the characteristics of the four software architectures for scheduling. (06 Marl

8 a. Write a major difference for the following topics
   i) Queues and Mailboxes
   ii) Ready and Running states
   iii) Encapsulating semaphores and encapsulating queues
   iv) Saving memory space and saving power. (08 Marl

b. What are semaphores? Explain the structure and use of binary semaphores for d protection. (06 Marl

c. Explain the 2 rules that the interrupt routines in a RTOS must follow. (06 Mar

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