2002 SCHEME

USN | | | | | | | | | | |

EC835

Eighth Semester B.E. Degree Examination, December 2010
Embedded System Design

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions.***
2. ***Standard notations are used.***
3. ***Missing data may be suitably assumed.***

1 a. What are the characteristics of an embedded system design? List the design metrics used to compare them. **(07 Marks)**

b. Determine the revenue loss, if the product's lifetime is 74 weeks and the delay in the market is 6 weeks. Derive the formula used for the calculation. **(07 Marks)**

c. For a particular product, determine the NRE cost and unit cost to be the following for the three listed IC technologies:
FPGA ($10000, $50): ASIC ($50000, $10)
VLSI ($200000, $5)
Determine the precise volumes for which each technology yields the lowest total cost. **(06 Marks)**

2 a. Develop an efficient algorithm for GCD. Convert it to FSMD and show the optimized FSMD. **(10 Marks)**

b. With a neat diagram, explain the architecture of a general purpose processor. **(10 Marks)**

3 a. Define the following: **(04 Marks)**
i) Cross compiler ii) Emulator iii) Debugger iv) In circuit simulator

b. Differentiate between:
i) Single purpose and general purpose processors
ii) Harvard and von-Neumann architecture **(06 Marks)**

c. With a neat diagram, explain how the pulse width modulator works. What are the considerations in selecting the clock, the prescalar and the counter? Assuming an 8-bit up counter, calculate the count to be loaded in the 'cycle-high' register to get pulses of duty cycle 75%. **(10 Marks)**

4 a. Given an analog input signal whose voltage ranges from 0 to 5 v and an 8-bit digital encoding, calculate the correct encoding for 3.5 v and then trace the successive approximation approach to find the correct encoding. **(08 Marks)**

b. What is cache mapping? Explain the direct mapping techniques for cache. **(08 Marks)**

c. Explain the terms write ability and storage permanence. **(04 Marks)**

5 a. Explain two level multibus architecture, with a neat diagram. **(06 Marks)**

b. Compose 1K× 8 ROMs into 2K × 16 ROM. **(06 Marks)**

c. Given the following three cache designs, find the one with the best performance, by calculating the average cost of access. Show all calculations.
i) 4K byte, 8-way-set associative cache, with a 6% miss rate; cache hit costs one cycle, cache miss costs 12 cycles
ii) 8K byte, 4-way-set associative cache with a 4% miss rate; cache hit costs 2 cycles, cache miss costs 12 cycles
iii) 16K byte, 2-way-set associative cache with a 2% miss rate; cache hit costs 3cycles, cache miss costs 12 cycles. **(08 Marks)**

6 a. What is interrupt latency? What are the factors affecting it? **(08 Marks)**

b. Explain with an example, how the Round-Robin architecture works. When is it not suitable? **(08 Marks)**

c. What is a reentrant function? Give the three rules to decide reentrant functions. **(04 Marks)**

7 a. What is semaphore? Explain RTOS semaphore. **(10 Marks)**

b. Differentiate between hard and soft RTOS highlighting the advantages and disadvantages of each. **(06 Marks)**

c. Explain 'deadly embrace'. **(04 Marks)**

8 a. What is an event? Give three standard features of an event. **(05 Marks)**

b. Give a comparison of methods for inter task communication. **(04 Marks)**

c. Explain the two rules, that the interrupt routines must follow, in RTOS environment. What is the effect of blocking on interrupts? Explain with a diagram. **(08 Marks)**

d. Explain the role of timer function in RTOS. **(03 Marks)**

* * * * *