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Seventh Semester B.E. Degree Examination, May/June 2010
DSP Algorithms and Architecture

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting
at least TWO questions from each part.**

PART – A

1.
 - a. Explain the issues to be considered in designing and implementing a DSP system, with the help of a neat block diagram. (06 Marks)
 - b. Briefly explain the major features of programmable DSPs. (06 Marks)
 - c. Explain the operation used in DSP to increase the sampling rate. The sequence $x(n) = [0, 2, 4, 6, 8]$ is interpolated using interpolation sequence $b_R = [1/2, 1, 1/2]$ and the interpolation factor is 2. Find the interpolated sequence $y(m)$. (08 Marks)
2.
 - a. What is the role of shifter in DSP? Explain the implementation of 4-bit shift right barrel shifter, with a diagram. (06 Marks)
 - b. Identify the addressing modes of the operands in each of the following instructions and their operation.
i) ADD B ; ii) ADD # 1234 h ; iii) ADD 5678 h ; iv) ADD + * addrreg. (08 Marks)
 - c. Explain the features of a program sequencer unit of a programmable DSP with a neat block diagram. (06 Marks)
3.
 - a. Describe the multiplier/adder unit of TMS 320 C 54 xx processor with a neat block diagram. (06 Marks)
 - b. Describe any four data addressing modes of TMS 320 C 54 xx DSP with examples. (08 Marks)
 - c. Assume that the current contents of AR3 to be 400 h, what will be its contents after each of the following TMS 320 C 54 xx addressing modes is used? Assume that the contents of ARO are 40 h.
i) * AR3 + 0 ; ii) * AR3 + ; iii) * AR3 + OB. (06 Marks)
4.
 - a. Describe the operation of the following instructions of TMS 320 C54 xx processor, with an example.
i) MAC ; ii) RPT ; iii) MPY. (06 Marks)
 - b. Describe the operation of hardware timer with a neat diagram. (06 Marks)
 - c. By means of a figure explain the pipeline operation of the following sequence of instruction if the initial values of AR1, AR3, A are 104, 101, 2 and the values stored in the memory locations 101, 102, 103, 104 are 4, 6, 8, 12. Also provide the values of registers AR3, AR1, T and accumulator after completion of each cycle.
ADD * AR3 + , A
LD * AR1 + , T
MPY * AR3 + , B
ADD B, A

(08 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.

PART – B

- 5 a. Describe the importance of Q-notation in DSP algorithm implementation, with examples. What are the values represented by 16 – bit fixed point number $N = 4000$ h in Q15, Q10, Q7 notations? (10 Marks)
- b. Explain how the FIR filter algorithms can be implemented using TMS 320 C54 xx processor. (10 Marks)
- 6 a. Explain a general DITFFT butterfly in place computation structure. (04 Marks)
- b. Determine the number of stages and number of butterflies in each stage and the total number of butterflies needed for the entire computation of 512 point FFT. (06 Marks)
- c. Explain how the bit-reversed index generation can be done in 8 point FFT. Also write a TMS 320 C 54 xx program for 8 point DIT FFT bit reversed index generation. (10 Marks)
- 7 a. Explain the memory interface block diagram for the TMS 320 C 54 xx processor. (06 Marks)
- b. Draw the I/O interface timing diagram for read – write – read sequence of operation. (06 Marks)
- c. What are interrupts? How interrupts are handled by the C 54 xx DSP processors. (08 Marks)
- 8 a. Explain with a neat diagram, the synchronous serial interface between the C54 xx and a CODEC device. (06 Marks)
- b. Explain the operation of Pulse Position Modulation (PPM) to encode two biomedical signals. (06 Marks)
- c. Explain with a neat block diagram, the operation of the pitch detector. (08 Marks)

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