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06EC56

Fifth Semester B.E. Degree Examination, May/June 2010
Fundamentals of CMOS VLSI

Time: 3 hrs. Max. Marks:100

Note: ***1. Answer any FIVE full questions, selecting at least TWO questions from each part.***
2. Draw neat diagrams.

PART – A

1 a. Explain the fabrication steps in P-well CMOS fabrication. **(10 Marks)**
b. Obtain the de transfer characteristics of a CMOS inverter and mark all the regions showing the status of PMOS and NMOS. **(10 Marks)**

2 a. Compare CMOS and bipolar technologies. **(04 Marks)**
b. Explain the transmission gate operation. **(04 Marks)**
c. Draw λ-based design rules for double metal CMOS process for layers and transistors. **(08 Marks)**
d. Draw the circuit diagram and stick diagram for nand gate. **(04 Marks)**

3 a. Explain different types of pseudo – NMOS logic. **(07 Marks)**
b. Explain CMOS domain logic and derive the evaluation voltage equation. **(08 Marks)**
c. Explain 2-input x-nor gate in pass transistor logic. **(05 Marks)**

4 a. Explain the terms : i) Rise time ; ii) Fall time ; iii) Delay time. Derive the equations for fall time of CMOS inverter. **(08 Marks)**
b. Provide scaling factors for gate area, gate delay, sat current. **(06 Marks)**
c. Explain in brief the wiring capacitances. **(06 Marks)**

PART – B

5 a. Explain the restoring logic, in detail. **(04 Marks)**
b. How to implement the switch logic for 4-way multiplexer? Explain. **(08 Marks)**
c. Explain the pre charge bus approach, used in system design. **(08 Marks)**

6 a. Explain the 4 x 4 cross bar switch operation. Mention the salient features of sub system design process. **(08 Marks)**
b. Explain the design steps for A 4-bit adder. **(06 Marks)**
c. How can 4-bit ALU architecture be used to implement an adder? **(06 Marks)**

7 a. Explain the read and write operations in dynamic memory cell. **(06 Marks)**
b. Explain booth multiplier, with an example. **(08 Marks)**
c. Explain different types of I/O pads. **(06 Marks)**

8 a. Write a note on testability and testing. **(10 Marks)**
b. Explain the ground rubs for a system design. **(10 Marks)**

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