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06ES33

Third Semester B.E. Degree Examination, June / July 08
Logic Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE questions, choosing atleast two from each part.***

PART - A

1 a. Simplify the following expression using Karnaugh Map. Implement the simplified circuit using the gates as indicated.
i) $f(ABCD) = \Sigma m(2,3,4,5,13,15) + \Sigma\alpha(8,9,10,11)$ use only NAND gates
ii) $f(ABCD) = \pi(2,3,4,6,7,10,11,12)$ use only NOR gates
to implement these circuits. **(12 Marks)**

b. Fig shows a BCD counter that produces a 4 –bit output representing the BCD code for the number of pulses that have been applied to the counter input. For example, after four pulses have occurred, the counter outputs are $(ABCD) = (0100)_2 = (04)_{10}$. The counter resets to 0000 on the tenth pulse and starts counting over again. Design the logic circuit that produces a HIGH output. Whenever the count is 2, 3 or 9. Use K – mapping and take advantages of "don't care" conditions. Implement the logic circuit using NAND gates.

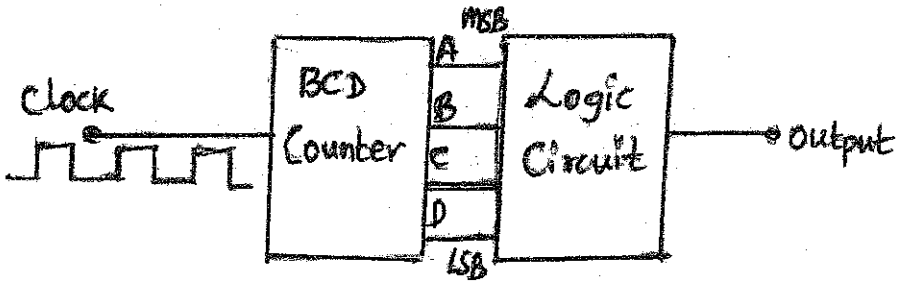

Fig. Q 1(b) **(08 Marks)**

2 a. Simplify the logic function given below, using Quine–McCluskey minimization technique. $Y(ABCD) = \Sigma m(0,1,3,7,8,9,11,15)$. Realize the simplified expression using universal gates. **(12 Marks)**

b. Simplify the logic function given below using variable – entered mapping (VEM) technique. $Y(ABCD) = \Sigma m(1,3,4,5,8,9,10,15) + \Sigma d(2,7,11,12,13)$. **(08 Marks)**

3 a. Realize the following Boolean function $f(ABCD) = \Sigma(0,1,3,5,7)$
Using – i) 8 : 1 MUX(74151) ii) 4 : 1 MIX(74153). **(08 Marks)**

b. Design a combinational logic circuit that will convert a straight BCD digit to an Excess – 3 BCD digits.
i) Construct the truth table
ii) Simplify each output function using Karnaugh Map and write the reduced equations.
iii) Draw the resulting logic diagram. **(12 Marks)**

4 a. Design a 4 – bit BCD adder circuit using 7483 IC chip, with self correcting circuit. i.e., a provision has to be made in the circuit, in case if the sum of the BCD number exceeds 9. **(12 Marks)**

b. Design a combinational circuit that accepts two unsigned 2 – bit binary number and provides 3 outputs.
Inputs : word $A = A_1A_0$, word $B = B_1B_0$.
Output : A = B, A>B, A<B. **(08 Marks)**

PART - B

5 a. Derive the characteristics equations of the following flip flops.
i) SR flip flops ii) JK flip flop. **(10 Marks)**

b. Explain clearly the operation of an asynchronous inputs in a flip flops with suitable example. **(06 Marks)**

c. An edge triggered 'D' flip flop is connected as shown in the Fig. Q 5(b). Assume that Q = 0 initially and sketch the wave form and determine its frequency of the signal at 'Q' output.

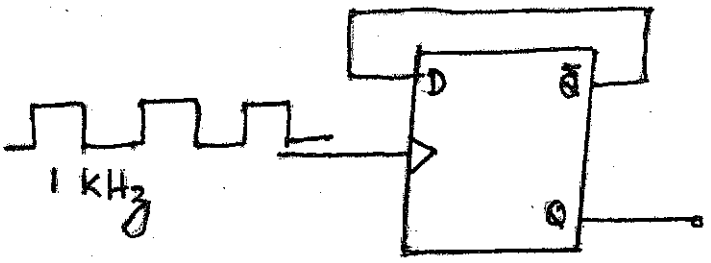

Fig. Q 5(C) **(04 Marks)**

6 a. With the help of a suitable example, explain the following operations in a shift register.
i) SISO ii) PISO iii) Twisted ring counter. **(10 Marks)**

b. Design a ripple counter to count the following sequence, 1111, 1110, 1101, 1100, 1011, 1111, 1110, 1101, 1100, 1011, etc. Suggest a suitable circuit using 7490 and other gates to obtain the desired result. **(10 Marks)**

7 a. With a suitable example, explain the Mealy and Moore Model of a sequential circuit. **(10 Marks)**

b. Construct the state table for the following state diagram.

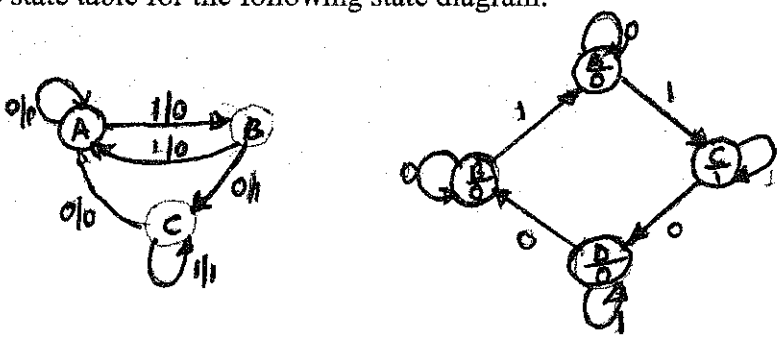

Fig. Q 7(c) **(10 Marks)**

8 a. Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D – flip flop.

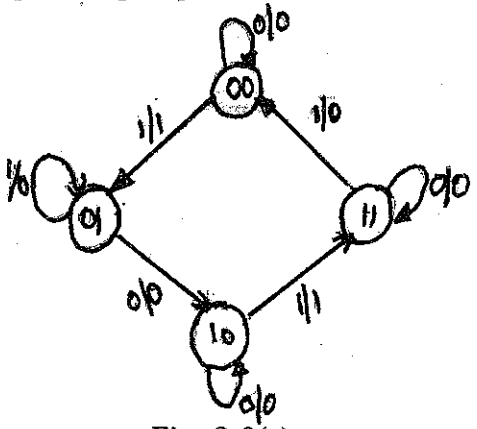

Fig. Q 8(a) **(12 Marks)**

b. Design a counter using JK – flip flops whose counting sequence is 000, 001, 100, 110, 111,101, 000 etc. by obtaining its minimal sum equations. **(08 Marks)**

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CS33

Third Semester B.E. Degree Examination, June / July 08
Logic Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Show that EX-OR operation is not distributive over AND operation. **(04 Marks)**

b. State and explain the Shannon's Reduction theorem. **(04 Marks)**

c. Find the conjuctive and Disjunctive canonical forms of the expression: F(ABC) = AC + BC' **(06 Marks)**

d. Realize the EX – NOR function using only minimum number of i) Nand Gates ii) NOR Gates. **(06 Marks)**

2 a. Define i) Subsume ii) Prime implicant iii) Essential prime implicant. Give an example for each. **(06 Marks)**

b. Find the minimal conjunctive normal form for f(ABCD) = A ◯ B ◯ C ◯ D. Use K maps for specification. **(08 Marks)**

c. For the given Boolean function, determine a minimal sum using variable entered maps where x, y and z are map variables. **(06 Marks)**

$f(ABxyz) = A\ \bar{x}\bar{y}\bar{z} + A\bar{x}\bar{y}z + Ax\bar{y}z + \bar{B}\bar{x}\bar{y}z + B\bar{x}y\bar{z} + \bar{x}yz + x\bar{y}\bar{z}$

3 a. Design a 4 input one output minimal gate combination network using only NAND GATES which has a 0 output when the majority of its inputs are at logic 1 and a 1 output when the majority of its inputs are logic 0. When the number of 1's and 0's are equal consider it as a don't care output. **(10 Marks)**

b. Design a stage of one Bit comparator which when cascaded helps in comparing two Binary numbers of any bit length. Draw the logic diagram. **(10 Marks)**

4 a. Design a full subtractor using 3 to 8 Decoder and Nand gates. **(10 Marks)**

b. Realize the two expression given $f_1(x\ y\ z) = \sum m(1, 2, 3, 7)$ and $f_2(x\ y\ z) = \sum m(0, 1, 2, 6)$. using PLA of the smallest size and draw the PLA table. **(10 Marks)**

5 a. What are the disadvantages of Totempole output? Draw and explain the logic diagram of a circuit, which removes the above disadvantage. **(10 Marks)**

b. Give a detailed comparison among LSTTL CMOS and ECL logic families highlighting the advantages of each for a given application. **(10 Marks)**

6 a. Draw a switch Debouncer using a SR latch and show the waveforms of switch Bounce and Debounce. **(10 Marks)**

b. Explain the advantages of an edge triggered flip flop over a pulse triggered flip-flop. **(04 Marks)**

c. Derive the characteristic equation of an SR flip flop and a JK flip flop. **(06 Marks)**

7 a. Design a Modulo – 6 self correcting counter whose counting sequence is 0 – 1 – 4 – 6 – 7 – 5 – 0. Use JK Flip Flops for realization. **(10 Marks)**

b. Draw the two forms of 3 bit shift register counters and explain their operation. **(10 Marks)**

8 a. Distinguish between Mealy and Moore model of clocked synchronous sequential network with block diagrams. **(08 Marks)**

b. State table shown refers to a clocked synchronous sequential network. Make a state assignment in binary code and find the excitation and output functions using JK flip flops. Draw the logic diagrams. **(12 Marks)**

PS	NS		Output	
	x = 0	x = 1	x = 0	x = 1
A	B	C	0	0
B	A	A	0	1
C	D	A	0	1
D	A	D	0	1

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06CS33

Third Semester B.E. Degree Examination, June / July 08
Logic Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions, choosing atleast two from each part.***

PART - A

1 a. What are universal gates? Implement the following function using universal gates only $\left(\overline{(A+B)C}\right)D$ **(04 Marks)**

b. Simplify the following using K – map $F(A,B,C,D) = \overline{A}\overline{B}C + AD + B\overline{D} + C\overline{D} + A\overline{C} + \overline{A}\overline{B}$. **(06 Marks)**

c. What are the drawbacks of k-map? Simplify the following expression using Quine – Mc Clusky Method. $F(A,B,C,D) = \Sigma(1,2,8,9,10,12,13,14)$. **(10 Marks)**

2 a. Show that using a 3 – to – 8 decoder and multi –input OR gate. The following Boolean expressions can be realized.
$F_1(A,B,C) = \Sigma m(0,4,6)$, $F_2(A,B,C) = \Sigma m(0,5)$, $F_3(A,B,C) = \Sigma m(1,2,3,7)$. **(04 Marks)**

b. Design Decimal – to – BCD encoder? **(04 Marks)**

c. What are the different types of PLD's and implement the 7 – segment decoder using PLA? **(08 Marks)**

d. Write a verilog code for 4 : 1 multiplexer using case statement. **(04 Marks)**

3 a. i) Perform 8 – bit addition of the decimal numbers – 28 and + 15 in 2's complement.
ii) Perform 8 – bit subtraction of the decimal numbers – 28 and + 65 in 2's complement. **(06 Marks)**

b. i) Find the binary addition of $(7510)_{10}$ and $(538)_{10}$ using 16 – bit numbers.
ii) Find the binary subtraction of $(200)_{10}$ and $(125)_{10}$ using 8 – bit numbers. **(10 Marks)**

c. Explain the binary Adder – subtracted circuit with an example. **(04 Marks)**

4 a. What is Schmitt trigger? Explain Schmitt trigger transfer characteristic. **(10 Marks)**

b. Explain the different types of flip fops along with their truth table. Also explain the race – around condition in a flip flop.

c. Differentiate between combinational circuit and sequential circuit. **(10 Marks)**

PART - B

5 a. Explain a 4 –bit serial input shift registers in detail and give its timing diagram. **(10 Marks)**

b. Design a mod – 5 synchronous up counter using JK flip flop. **(10 Marks)**

6 a. Explain Moore model with state synthesis table and also obtain the circuit diagram for Moore model. **(10 Marks)**

b. Design an asynchronous sequential logic circuit for state transition diagram shown in Fig. Q 6(b).

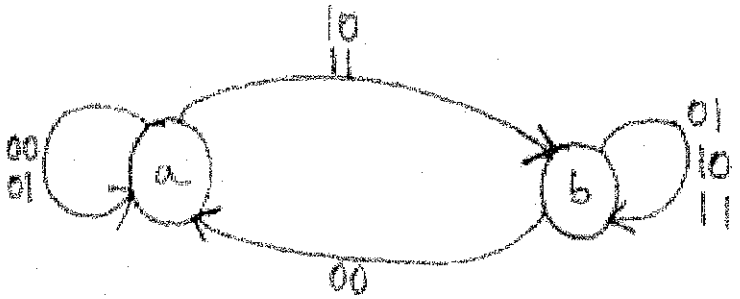

Fig. Q 6(b) **(10 Marks)**

a. What is a binary ladder? Explain the binary ladder with a digital input of 1000. **(10 Marks)**

b. Explain a 2 – bit simultaneous A/D converter. **(10 Marks)**

a. With a circuit diagram, explain the operation of the CMOS NAND gate. **(10 Marks)**

b. Explain a 2 – input NAND gate TTL with Totem – pole output with a neat diagram. **(10 Marks)**

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06CS33

Third Semester B.E Degree Examination, Dec. 07 / Jan. 08
Logic Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions choosing at least TWO questions from each part..***

PART – A

1 a. Using Karnaugh map simplify the following Boolean expression and give the implementation of the same using :
i) NAND gates only (SOP form) ii) NOR gates only (POS form)
$f(A, B, C, D) = \sum m\ (0, 1, 2, 4, 5, 12, 14) + dc\ (8, 10)$. **(08 Marks)**

b. Find the prime implicantes for the Boolean expression using Quine Mc Clusky's method.
$F(w, X, Y, Z) = \sum m\ (1, 3, 6, 7, 8, 9, 10, 12, 13, 14)$. **(10 Marks)**

c. Explain the principle of duality. **(02 Marks)**

2 a. Realize the Boolean expression $f(w, x, y, z) = \sum m(4, 6, 7, 8, 10, 12, 15)$ using a 4 to 1 line multiplexer and external gates. **(08 Marks)**

b. Design a 1-bit comparator using basic gates. **(05 Marks)**

c. Implement the following Boolean functions using an appropriate PLA.
$F1(A, B, C) = \sum m(0, 4, 7)$; $F2(A, B, C) = \sum m(4, 6)$. **(04 Marks)**

d. What are the three different models for writing a module body in Verilog HDL. Give an example for any one model. **(03 Marks)**

3 a. Explain with example the 2's complement arithmetic using all the cases. **(04 Marks)**

b. Draw a block diagram of a 4 – bit adder – subtract circuit using full adder and give a brief description. **(04 Marks)**

c. Design a 2-bit fast adder. Give its implementation using gates. **(08 Marks)**

d. Write a HDL code for a full adder. **(04 Marks)**

4 a. Write the characteristic of an ideal clock. **(06 Marks)**

b. With the help of a block diagram, explain the working of a JK Master – Slave flip – flop. **(08 Marks)**

c. Show how a SR flip – flop can be converted to a JK flip – flop. **(06 Marks)**

PART – B

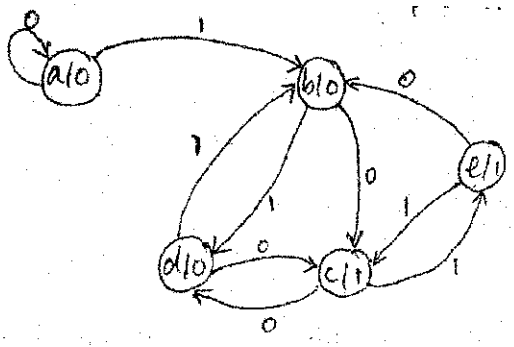
5 a. Distinguish between a ring counter and a Johnson counter. **(04 Marks)**

b. Explain the working of a 3-bit asynchronous down counter. **(06 Marks)**

c. Design a synchronous mod – 5 up counter using JK flip – flop. Give excitation table of JK flip – flop, state diagram and state table. **(10 Marks)**

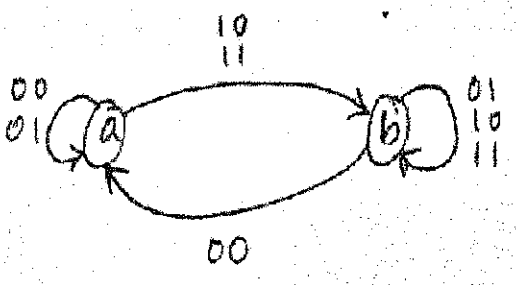
6 a. Explain the difference between Mealy and Moore models. **(04 Marks)**

b. Reduce the state transition diagram by row elimination method and implication table method.



(10 Marks)

c. Design an asynchronous sequential logic circuit for the state transition diagram shown. **(06 Marks)**



7 a. Draw a 4-bit D/A converter using R/2R resistors and explain its working. **(10 Marks)**

b. Explain the A/D converter by simultaneous conversion. Draw the block diagram of a 2 – bit simultaneous A/D converter. **(10 Marks)**

8 a. With the aid of a circuit diagram, explain the operation of a 2 – input TTL NAND gate with totem – pole output. **(08 Marks)**

b. Explain the operation of a 2 – input CMOS NOR gate with a help of a circuit diagram. **(06 Marks)**

c. Write a note on the CMOS characteristics. **(06 Marks)**

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CS33

Third Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Logic Design

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. With suitable example explain: i) Boolean function ii) Maximum canonical formula iii) Incomplete Boolean function. **(06 Marks)**

b. Show the realization of the following:
i) NOR using NAND gates ii) X-NOR using NAND gates. **(10 Marks)**

c. Draw the logic diagram using basic gates of the following Boolean function:
$f(A,B,C,D) = \overline{A(B(CD+\overline{E})+\overline{CE})} + \overline{A}\,\overline{B}$ assuming input variables are available in uncomplemented and complemented form. **(04 Marks)**

2 a. Differentiate between positive, negative and mixed logic. Give example for each case. **(06 Marks)**

b. Prove that: i) $x + \bar{x}y = x + y$ ii) $ab + \overline{ac} + a\bar{b}c(ab + c) = 1$. **(08 Marks)**

c. Simplify using Karnaugh map method and realize the simplified function using NAND gates.
$f(x,y,z) = \sum m(0,1,4) + \sum dc(3,7)$. **(06 Marks)**

3 a. Design a minimal two level gate combinational network that detects the presence of six illegal code group in a 4-bit that represent 8421 BCD code, by providing logic 1 output. **(10 Marks)**

b. Simplify the following switching function using Quine-Mccluskey method:
$f(A,B,C,D) = \sum m(1,3,13,15) + \sum dc(8,9,10,11)$. **(10 Marks)**

4 a. Define: i) Propagation delay ii) Power-delay product iii) Fan-out iv) Noise margin. **(04 Marks)**

b. Write the circuit diagram of a TTL NAND gate and draw and explain the transfer characteristic. **(07 Marks)**

c. Explain with respect to TTL the following output stages:
i) Totem pole ii) Open collector iii) Tri-state output. **(09 Marks)**

5 a. Draw the circuit of a JK-flipflop using NAND gates building blocks. Verify that JK-flipflop satisfy the difference equation: $Q_{n+1} = J_n\overline{Q}_n + \overline{K}_nQ_n$. **(10 Marks)**

b. Show how JK-flipflop can be connected as i) D-flipflop ii) T-flipflop. **(06 Marks)**

c. Describe a C-MOS inverter with relevant circuit diagram. **(04 Marks)**

6 a. Differentiate between ripple and synchronous counter. **(04 Marks)**

b. Design a synchronous module-S counter and sketch the output waveform. **(08 Marks)**

c. With a block diagram describe a 3-bit Johnson twisted ring counter. Draw the sequence diagram and indicate the valid and invalid states. **(08 Marks)**

7 a. Discuss what is race – around in JK-flipflop and describe: i) Master – slave JK-flipflop ii) Edge triggered flipflop. **(12 Marks)**

b. Design suitable circuit for the output of truth table shown in the table below using i) 8:1 Multiplexer ii) 4:1 Multiplexer. **(08 Marks)**

Inputs			Outputs
A	B	C	D
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	0
1	1	1	0

8 Write short notes on any three of the following:
a) Priority encoder b) CMOS in comparison with TTL family c) Magnitude comparator
d) Programmable array logic. **(20 Marks)**

06ES33

Third Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Logic design

ıe: 3 hrs. Max. Marks:100

Note : *1. Answer any FIVE full questions.*
2. Assume missing data if any suitably.

a. Two motors M_2 and M_1 are controlled by three sensors S_3, S_2 and S_1. One motor M_2 is to run any time all three sensors are on. The other motor is to run whenever sensors S_2 or S_1 but not both are on and S_3 is off. For all sensor combinations where M_1 is on, M_2 is to be off except when all the three sensors are off and then both motors must remain off. Construct the truth table and write the Boolean output equation. **(06 Marks)**

b. Simplify using Karnaugh map. Write the Boolean equation and realize using NAND gates. $D = f(w,x,y,z) = \Sigma(0,2,4,6,8) + \Sigma d(10,11,12,13,14,15)$. **(06 Marks)**

c. Simplify $P = f(a,b,c,) = \Sigma(0,1,4,5,7)$ using two variable Karnaugh map. Write the Boolean equation and realize using logic gates. **(08 Marks)**

a. Simplify using Karnaugh map $L = f(a,b,c,d) = \pi(2,3,4,6,7,10,11,12)$ **(06 Marks)**

b. Simplify using Quine Mc Cluskey tabulation algorithm-
$V = f(a,b,c,d) = \Sigma(2,3,4,5,13,15) + \Sigma d(8,9,10,11)$ **(14 Marks)**

a. Design a combinational circuit that will multiply two two-bit binary values. **(08 Marks)**

b. Design a 4 to 16 decoder using two 3 to 8 decoder (74LS138). **(06 Marks)**

c. Design a keypad interface to a digital system using ten line BCD encoder (74LS147). **(06 Marks)**

a. Design a binary full subtractor using minimum number of gates. **(06 Marks)**

b. Explain the terms
i) Ripple – carry propagation
ii) Propagation delay
iii) Look- ahead carry
iv) Iterative design. **(04 Marks)**

c. Realize $F = f(x,y,z,) = \Sigma(1,2,4,5,7)$ using 8 – to – 1 multiplexer (74LS151). **(04 Marks)**

d. Design a two bit binary magnitude comparator. **(06 Marks)**

a. Explain with timing diagram the working of a S. R latch as a switch debouncer. **(06 Marks)**

b. Explain the working of a Master – slave JK Flip-Flop with functional table and timing diagram. Show how race around condition of master-slave SR Flip-Flop is over come. **(08 Marks)**

c. What is the significance of edge triggering? Explain the working of edge triggered D-flip-flop and T-flip-flop with their functional table. **(06 Marks)**

a. Obtain the characteristic equation for a SR flip-flop **(04 Marks)**

b. With a neat circuit diagram, explain the working of a universal shift register. **(08 Marks)**

c. Design a synchronous Mod-6 counter using clocked J K flip-flop. **(08 Marks)**

7 a. Explain mealy and Moore sequential circuit models. **(04 Marks)**

b. For the state machine M_1 shown in Fig. Q 7(b), obtain

i) State table

ii) Transition table

iii) Exaltation table for T flip-flop

iv) Logic circuit for T exaltation realization.

(16 Marks)

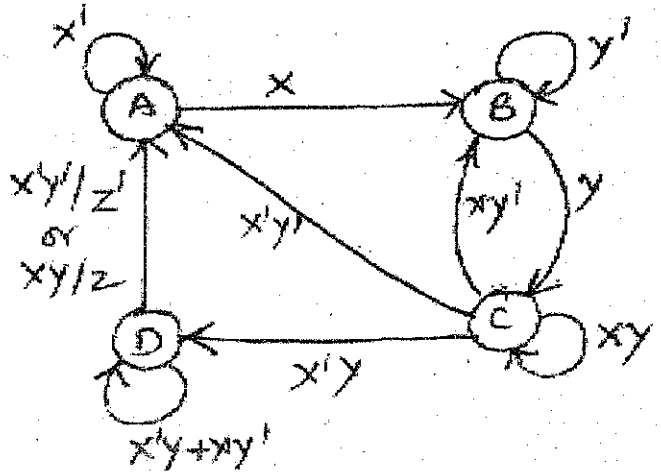

Fig. Q 7(b)

8 a. Construct a mealy state diagram that will detect a serial sequence of 10110. When the input pattern has bee detected, cause an output Z to be asserted high. **(08 Marks)**

b. Design a cyclic modulo-8 synchronous counter using J–K flip-flop that will count the number of occurrences of an input; that is, the number of times it is a 1. The input variable X must be coincident with the clock to be counted. The counter is to count in binary. **(12 Marks)**

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CS33

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NEW SCHEME

Third Semester B.E. Degree Examination, July 2007
CS / IS / EE / EC / IT / TC / BM / ML
Logic Design

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Using the theorems of Boolean algebra, simplify the following:

i) $y_1 = D(\overline{A} + B) + \overline{B}(C + AD)$

ii) $y_2 = \overline{\overline{A\overline{B}} + ABC + A(B + A\overline{B})}$

iii) $y_3 = \overline{A}\overline{B}\overline{C} + \overline{A}B\overline{C} + A\overline{B}\overline{C} + AB\overline{C}$ **(09 Marks)**

b. Express the following expressions in canonical form:

i) $y_1 = (A + B)(A + C)(B + \overline{C})$

ii) $y_2 = AC + AB + BC$ **(06 Marks)**

c. Give the implementation of EXOR gate using minimum number of NAND gates only. **(05 Marks)**

2 a. i) Express the following min term expression in POS form:
$y(A, B, C, D) = \Sigma m(1, 3, 5, 6, 7, 9, 10, 12, 15)$
ii) Express the following max term expression in SOP form:
$y(A, B, C) = \pi M(0, 3, 5, 6)$. **(06 Marks)**

b. i) What are the advantage, disadvantages of K map?
ii) Simplify the following function in SOP form using K Map:
$f(A, B, C, D) = \overline{A}BC + AD + B\overline{D} + C\overline{D} + A\overline{C}$ **(08 Marks)**

c. Simplify the following function in POS form using K map:
$f(A, B, C, D) = \pi M(0, 1, 2, 5, 8, 9, 10)$. **(03 Marks)**

d. Simplify the following function in SOP form using K map:
$y(w, x, y, z) = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$. **(03 Marks)**

3 a. Minimize the expression using Quine Mc Cluskey method.
$y(A, B, C, D) = \Sigma m(1, 2, 3, 5, 9, 12, 14, 15) + \Sigma d(4, 8, 11)$. **(10 Marks)**

b. Simplify the following using VEM technique. Reduce 4 variables to 3 variables.
$y = \overline{A}\overline{B}\overline{C}D + \overline{A}B\overline{C}D + A\overline{B}\overline{C}D + A\overline{B}CD + \overline{A}\overline{B}CD + \overline{A}BC\overline{D} + ABCD + ABC\overline{D}$ **(05 Marks)**

c. Realize a full adder using minimum number of 2 input NAND gates. Write the truth table, relevant expressions and logic diagram. **(05 Marks)**

4 a. Define the following:
i) Fan in and fan out
ii) Noise margin
iii) Propagation delay. **(06 Marks)**

b. Explain the operation of basic TTL NAND gate circuit with relevant diagram. **(07 Marks)**

c. Draw and explain the circuit of 2 input CMOS NOR gate. **(07 Marks)**

Contd.... 2

5 a. What is a magnitude comparator? Design a 2 bit digital comparator by writing the truth table, the relevant expression, and logic diagram. **(10 Marks)**

b. Implement the following Boolean function using 8:1 MUX:
F(A, B, C, D) = Σm(1, 2, 5, 9, 10, 14) **(06 Marks)**

c. Write the truth table of the following flip flops:
D, T, SR, JK. **(04 Marks)**

6 a. Write the excitation table of SR flip flop. Design a synchronous MOD-6 counter using SR flip flop for the following count sequence 0, 1, 3, 2, 6, 4 and repeat. Write the transition table, logic diagram. **(10 Marks)**

b. What is a look-ahead carry adder? Explain the circuit and operation of a 4 bit binary adder with look-ahead carry. **(10 Marks)**

7 a. Realize a 3 bit binary synchronous up counter using JK flip flop. Write the excitation table, transition table and logic diagram. Include preset, clear option. **(10 Marks)**

b. Explain the different types of shift register. SISO, SIPO, PIPO, PISO with relevant circuit diagram. **(10 Marks)**

8 a. A combinational circuit is defined by the functions:
$F_1 = \Sigma m(3, 5, 7)$
$F_2 = \Sigma m(4, 5, 7)$
Implement the circuit with a PLA having 3 inputs, 3 product terms and 2 outputs. **(08 Marks)**

b. A sequential network has one input and one output. The state diagram is shown in fig.8(b). Design the sequential circuit with T flip flop. **(12 Marks)**

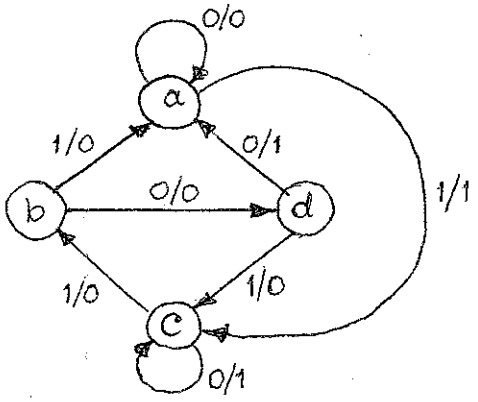

Fig.8(b)

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CS33

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NEW SCHEME

Third Semester B.E. Degree Examination, Dec. 06 / Jan. 07
EC / EE / IT / BM / ML / CS / IS
Logic Design

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Prove the following :
   i) $\overline{ac} + \overline{a}b + \overline{a}c + ab = a\overline{b}$
   ii) $(a + b)(\overline{ac} + c)(\overline{b + ac}) = \overline{a}b$
   iii) $a\overline{b} + b\overline{c} + \overline{a}c = \overline{a}b + \overline{b}c + a\overline{c}$ **(10 Marks)**

   b. Implement
   i) $w = x\overline{y} + \overline{x}y$ using NAND gates
   ii) $w = (x + z)(\overline{y} + v)(\overline{w} + \overline{x} + \overline{y})$ using NAND **(06 Marks)**

   c. Simplify using Boolean algebra
   $\overline{w}\overline{x}\overline{y}z + w\overline{x}\overline{y}z + xz + xy\overline{z}$ **(04 Marks)**

2 a. Identify all prime implicants and essential prime implicants of the following functions using K map.
   i) $f(a, b, c, d) = \Sigma m(0,1,2,5,6,7,8,9,10,13,14,15)$
   ii) $f(a, b, c, d) = \Pi m(0,2,3,8,9,10,12,14)$ **(08 Marks)**

   b. Find a minimal sum for the following Boolean function using Quine McCluskey method and prime-implicant table reduction
   $f(a, b, c, d) = \Sigma m(3,4,5,7,10,12,14,15) + \Phi(2)$ **(12 Marks)**

3 a. Find the minimal sum and minimal product using MEV technique using a,b,c as map variables
   $f(a, b, c, d) = \Sigma m(3,4,5,7,8,11,12,13,15)$ **(08 Marks)**

   b. Find minimal sum and minimal product for the following function using K-map
   $f(a, b, c, d) = \Sigma m(6,7,9,10,13) + dc(1,4,5,11,15)$ **(08 Marks)**

   c. Define :
   i) Positive logic
   ii) Negative logic **(04 Marks)**

4 a. With diagram, define
   i) Rise time
   ii) Fall time
   iii) Propagation delay
   iv) Fan-in
   v) Fan out. **(10 Marks)**

   b. Using NMOS draw the circuit for
   i) Inverter
   ii) NOR gate
   iii) NAND gate **(06 Marks)**

   c. Draw the circuit diagram for
   i) 2-input CMOS NOR
   ii) 2-input CMOS NAND **(04Marks)**

Contd.... 2

5 a. Construct 16:1 multiplexer using 4 tol and 2 tol multiplexer. **(04Marks)**

b. Implement the following using 4×4 PROM

Input (a, b)		Output (f_0, f_1, f_2, f_3)			
0	0	0	0	1	1
0	1	0	1	0	0
1	0	0	1	0	0
1	1	1	1	0	0

(04 Marks)

c. Implement $f(a,b,c,d) = \Sigma m(0,1,5,6,7,9,10,15)$ using

i) 8:1 MUX with a,b,c as select lines

ii) 4:1 MUX with a,b as select lines **(06 Marks)**

d. Design a 4 bit parallel fast look a head carry generator. **(06 Marks)**

6 a. Design a synchronous counter using JK flip flops to count in the sequence 0, 1, 2, 4, 5, 6, 0, 1, 2 . . . .
use state diagram and state table. **(08 Marks)**

b. Explain TTL with

i) Wired logic

ii) Open collector

iii) Totem pole output **(12 Marks)**

7 a. Give the logic diagram of

i) SR latch

ii) Gated D latch

iii) Master Slave JK flip flop

iv) Master Slave SR flip flop **(08 Marks)**

b. With diagram explain universal shift register. **(08 Marks)**

c. Explain the working of switch debouncer using SR latch. **(04 Marks)**

8 Write short notes on :

a. Ripple counter

b. PLA

c. Ring counter

d. Decoder. **(20 Marks)**

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CS 33

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NEW SCHEME

Third Semester B.E Degree Examination, July 2006
CS / IS / EC / TE / EE / IT / ML / BM
Logic Design

Time: 3 hrs.] [Max. Marks: 100

Note: *1. Answer any FIVE full questions.*

1 a. State and explain with examples shannon's expansion and reduction theorems in Boolean algebra. **(04 Marks)**

b. Simplify the following using Boolean theorems:

i) $f(x, y, z) = (x + y)[\overline{x}(\overline{y} + \overline{z})] + \overline{x}\overline{y} + \overline{x}\overline{z}$

ii) $f(A, B, C) = (A + B + C)(\overline{A} + B + C)(\overline{A} + B + \overline{C})$ **(08 Marks)**

c. Transform each of the following canonical expressions into other canonical form in decimal notation and express in simplified form in decimal notation and express in simplified form

i) $f(x, y, z) = \sum m(0, 1, 3, 4, 6, 7)$

ii) $f(w, x, y, z) = \prod m(0, 1, 2, 3, 4, 6, 12)$ **(08 Marks)**

2 a. What are don't care condition? What are its advantages? **(04 Marks)**

b. Obtain a NOR-gate realization of the Boolean expression, $f(w, x, y, z) = \sum m(0, 3, 5, 6, 9, 10, 12, 15)$ **(08 Marks)**

c. Obtain a NAND-gate realization of the Boolean expression $f(A, B, C) = (A + \overline{B} + C)(\overline{A} + \overline{B} + \overline{C})(\overline{A} + B)$ **(08 Marks)**

3 a. Determine the minimal sum-of-product (SOP) expression for $f(w, x, y, z) = \sum(0, 2, 4, 9, 12, 15) + \sum d(1, 5, 7, 10)$ **(08 Marks)**

b. Using Quine-Mcluskey method and prime implicant reduction, determine the minimal product-of-sums (POS) expression for the following using decimal notation $f(w, x, y, z) = \sum m(1, 2, 3, 5, 9, 12, 14, 15) + \sum d(4, 8, 11)$ **(08 Marks)**

c. Reduce the given switching function using single variable map technique $f(A, B, C, D) = \sum m(0, 1, 4, 7, 10, 14)$ **(04 Marks)**

4 a. Define the following terms:

i) Fan-in and Fan-out ii) The propagation delay **(06 Marks)**

b. What is the principle of operation of an schottky TTL? Explain with a circuit diagram the operation of a schottky TTL **(08 Marks)**

c. A TTL gate is generated to sink 10mA without exceeding an output voltage VOL=0.4V and to source 5mA without dropping below VOH = 2.4V. If I_{1H} =100mA at 2.4V and I_{1H} = 1mA at 0.4V, calculate the 0-state and 1-state fan-outs. **(06 Marks)**

5 a. With a block diagram describe the principle of operation of a carry Look-ahead-adder. **(06 Marks)**

b. What is a Programmable LOGIC Array (PLA)? Describe with a logic diagram the principle of operation of a PLA. What are its advantages? **(08 Marks)**

c. Implement the following Boolean function using 8:1 multiplexer. $F(A, B, C, D) = \overline{A}B\overline{D} + ACD + \overline{B}CD + \overline{A}\overline{C}D$. **(06 Marks)**

Contd....2

6 a. What is a sequential circuit? Discuss the different types of sequential circuits. **(06 Marks)**

b. With a neat logic diagram and timing waveforms describe the operation of a master-slave JK flip-flop. **(06 Marks)**

c. A stable assignment table for a mod-5 counter is given below:

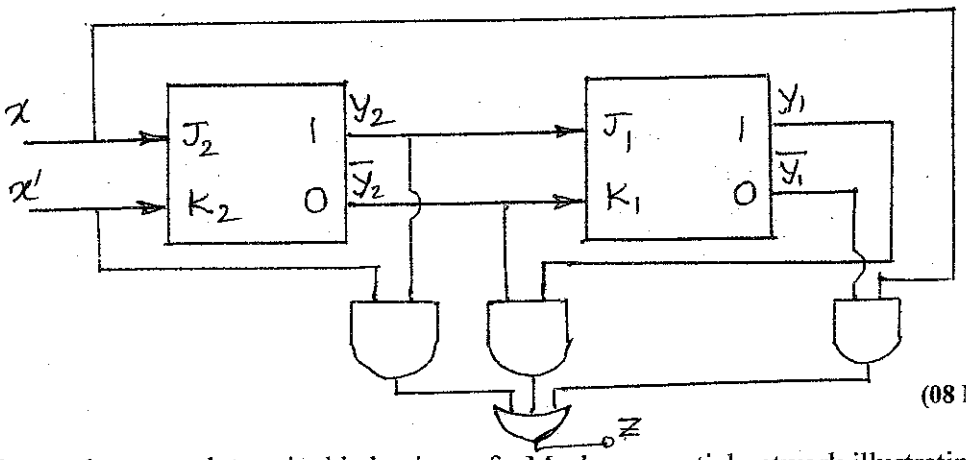
S	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	1
3	1	1	1
4	1	1	0

Derive a counter configuration. **(08 Marks)**

7 a. Explain with sketches the Mealy model and the Moore model sequential networks. **(06 Marks)**

b. Analyze the synchronous circuit of the Fig. (clock not shown but is implicit)

i) Write down the excitation and output functions
ii) Form the excitation and state tables
iii) Give a word description of the circuit operatin.



(08 Marks)

c. Discuss the network terminal behaviour of a Mealy sequential network illustrating the occurrence of false output with timing diagrams. **(06 Marks)**

8 Write short notes on:

i) Principle of duality
ii) Compansion of logic families
iii) CMOS inverter
iv) Programmable Read-only memories. **(20 Marks)**

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NEW SCHEME

CS33

Reg. No. | | | | | | | | | | |

Third Semester B.E. Degree Examination, January/February 2006

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs.) (Max.Marks : 100

Note: *1.Answer any FIVE full questions.*
2.All questions carry EQUAL marks.

1. **(a)** Prove the following consensus laws using Boolean postulates.

i) $xy + yz + \overline{x}z = xy + \overline{x}z$

ii) $(x+y)\,(y+z)\,(\overline{x}+z) = (x+y)\,(\overline{x}+z)$ **(4 Marks)**

(b) Prove that if $\overline{w}x + y\overline{z} = 0$ then

$$wx + \overline{y}(\overline{w} + \overline{z}) = wx + xz + \overline{x}\,\overline{z} + \overline{w}\quad \overline{y}z$$ **(6 Marks)**

(c) Mention the different methods available for manipulating Boolean formulas. Explain any three in detail. **(10 Marks)**

2. **(a)** Using graphical procedure, obtain a nor-gate realization of the Boolean expression

$$f(w,\ x,\ y,\ z) = \overline{w}z + w\overline{z}(x + \overline{y})$$ **(6 Marks)**

(b) Show that $A \odot B \odot C \odot D = \sum m(0,\ 3,\ 5,\ 6,\ 9,\ 10,\ 12,\ 15)$ **(4 Marks)**

(c) Using Karnaugh maps, determine the minimal sums and minimal products for

$$f(w,\ x,\ y,\ z) = \sum m\,(0,\ 1,\ 3,\ 7,\ 8,\ 12) + dc(5,\ 10,\ 13,\ 14)$$

Is your answer unique? **(10 Marks)**

3. **(a)** Using the Quine-Mccluskey method and prime implicant table reductions, determine the minimal sums for the incomplete Boolean function

$$f(v,\ w,\ x,\ y,\ z) = \sum m(4,\ 5,\ 9,\ 11,\ 12,\ 14,\ 15,\ 27,\ 30) + dc(1,\ 17,\ 25,\ 26,31)$$ **(10 Marks)**

(b) Explain the procedure for loading a K-map using map entered variable technique. Write the map entered variable K-map for the Boolean function.

$$f(w,\ x,\ y,\ z) = \sum m(2,\ 9,\ 10,\ 11,\ 13,\ 14,\ 15)$$ **(10 Marks)**

4. **(a)** Explain the operation of a two input TTL nand-gate with totem-pole output with a neat circuit diagram. **(8 Marks)**

(b) What is a FET? Explain how to construct a resistor with the n-channel, enhancement type MOSFET. **(6 Marks)**

(c) Explain with the help of a circuit diagram the operation of a two input CMOS nor-gate. **(6 Marks)**

5. **(a)** Explain a 4-bit parallel adder with carry lookahead scheme. **(10 Marks)**

(b) What is an encoder? Explain an 8-to-3 line encoder. **(4 Marks)**

Contd.... 2

(c) Implement a full adder circuit with a 3-to-8 line decoder and two OR gates. **(6 Marks)**

6. (a) Implement the following Boolean function with an 8 x 1 multiplexer with A, B and D connected to selection lines S_2, S_1, and S_0 respectively.

$$F(A, B, C, D) = \sum m(0, 1, 3, 4, 8, 9, 15)$$ **(6 Marks)**

(b) Implement the following Boolean expressions using a PROM.

$$f_1(x_2, x_1, x_0) = \sum m(0, 1, 2, 5, 7)$$

$$f_2(x_2, x_1, x_0) = \sum m(1, 2, 4, 6)$$ **(6 Marks)**

(c) Explain the different types of flipflops along with their truth table. Also explain the race-around condition in a flipflop. **(8 Marks)**

7. (a) Design a synchronous mod-3 counter with the following binary sequence using clocked JK flipflops.

Count sequence : 0, 1, 2, 0, 1, 2, ... **(10 Marks)**

(b) Explain the Mealy model and Moore model of a clocked synchronous sequential network. **(10 Marks)**

8. Write short notes on :

a) Implies and subsumes

b) Fan-in and Fan-out

c) Universal shift register

d) Programmable logic arrays **(4×5=20 Marks)**

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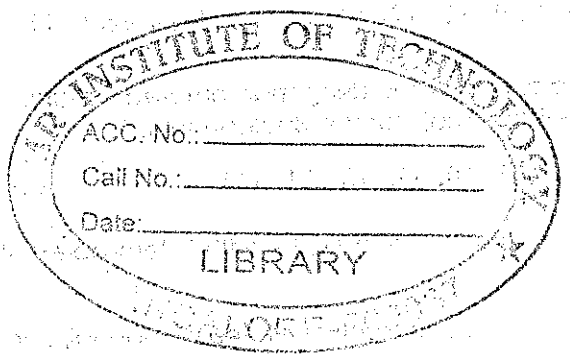

NEW SCHEME

CS33

USN | | | | | | | | | | |

Third Semester B.E. Degree Examination, January/February 2005

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs.] [Max.Marks : 100

Note: *1.Answer any FIVE full questions.*
2.All questions carry EQUAL marks.

1. (a) Explain the principle of duality in Boolean algebra. Write the duals of the following Boolean theorems:

i) $a + b + ab = a + b$

ii) $a + b + \overline{a}\,\overline{b} = 1$

iii) $ab + bc + \overline{c}a = bc + \overline{c}a$ (8 Marks)

(b) Complement the following Boolean expressions and write them as the sum of minterms.

i) $\overline{a} + \overline{b} + \overline{c} + \overline{d}$

ii) $ab + \overline{(abcd)}$ (6 Marks)

(c) Rewrite the following Boolean expressions in the M-notation and simplify :

i) $(a + b)(a + c)$

ii) $(a + b)(b + c)(\overline{c} + a)$ (6 Marks)

2. (a) What ia a universal gate? Consider a gate which takes two inputs A and B and produces an output $\overline{A} \cdot B$. Would you consider it a universal gate? Discuss. (10 Marks)

(b) Get the minimised sum-of products expression for

$f(a, b, c, d) = \sum m(0, 1, 5, 6, 7, 8, 9)$

with don't cares : $\sum m(10, 11, 12, 13, 14, 15)$

Use Karnaugh map for simplification. (10 Marks)

3. (a) Give the truth table for a binary full adder function and obtain the irredundant disjunctive normal expression for the function. Show how the function could be realised using NAND gates. (10 Marks)

(b) Use Quine McCluskey method and simplify the following function : $f(a, b, c, d) = \sum m(0, 1, 2, 3, 8, 9)$ (10 Marks)

4. (a) Explain the following properties of integrated circuits of the SSI type (small scale integration type)

i) Propagation delay

ii) Noise margin

iii) Fan - in

iv) Fan-out

Compare TTL and CMOS gates, in respect of these properties. (10 Marks)

(b) With a circuit diagram, explain the operation of the CMOS NAND gate. What are its advantages over corresponding TTL gates? (10 Marks)

Contd.... 2

5. (a) Explain clearly the Totem pole output stage and the Three-state output stage of a TTL gate. When would the three state stage be useful? (10 Marks)

   (b) What is a look-ahead carry adder? Explain the circuit and operation of a 4-bit binary adder with look-ahead carry. (10 Marks)

6. (a) How would you realise the function

   $ABCD + \overline{A}BC + B\overline{C}\ \overline{D}$ using an 8-to -1 multiplexer? (10 Marks)

   2v (b) Distinguish between PLA and PAL. Show how you would realise a Boolean function using a PLA. (10 Marks)

7. (a) Explain the operation of a simple SR flip flop using NAND gates. (10 Marks)

   (b) Draw the circuit and explain a synchronous mod-6 counter using J-K flipflops. (10 Marks)

8. Design a sequential machine using D-flipflops for realising the state table below. The machine is of a single input single output type.

Present state	Next state for input x=		Output Z for input x=	
	0	1	0	1
A	B	C	0	0
B	A	A	0	1
C	D	A	0	1
D	A	D	0	1

Indicate the state transition diagram. Does the state assignment. Work out the excitation and the output logics? (20 Marks)

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NEW SCHEME

CS33

USN | | | | | | | | | | |

Third Semester B.E. Degree Examination, July/August 2005

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*

1. (a) Explain Demorgan's theorems in Boolean Algebra. (4 Marks)

   (b) State and explain two applications of shift register. (6 Marks)

   (c) Design a combinational circuit for 3 bit even-parity generator and implement it using NAND gates only. (10 Marks)

2. (a) Design BCD to Excess 3 code converter using NOR gates only. (8 Marks)

   (b) What is race around condition? Explain how it is eliminated using J-K master-slave flip-flop. (12 Marks)

3. (a) Using Quine Mc Clusky tabulation method, obtain the set of prime implicants for the function

   $$f(a,b,c,d) = \sum(0,1,4,5,9,10,12,14,15) + \sum\phi(2,8,13)$$

   and hence obtain the minimal form of the given function employing decimal representation. (12 Marks)

   (b) Design mod-4 ripple up counter with initial state is $(011)_2$. Draw timing diagram for the same. (8 Marks)

4. (a) Simplify the following using VEM technique. Reduce 4 variables to 3 variables

   $$Y = \overline{A}\,\overline{B}\,\overline{C}\,\overline{D} + \overline{A}\,\overline{B}\,\overline{C}\,D + A\,\overline{B}\,\overline{CD}$$
   $$+A\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}\,C\,D + \overline{A}\,B\,C\overline{D} + A\,B\,C\,D + A\,B\,C\overline{D}$$

   Implement it using AOI logic. (8 Marks)

   (b) Define fan-in and fan out - (4 Marks)

   (c) Explain a two input NAND gate TTL with totem pole output with a neat circuit diagram. (8 Marks)

5. (a) Design 3:8 active low output decoder. (7 Marks)

   (b) Compare Moore and Meelay models. (8 Marks)

   (c) Construct 8:1 multiplexer using 2:1 multiplexer. (5 Marks)

6. (a) Implement the following multi Boolean function using $3 \times 4 \times 2$ PLA PLD

   $f_1(a_2,a_1,a_0) = \sum m(0,1,3,5)$ and
   $f_2(a_2,a_1,a_0) = \sum m(3,5,7)$ (8 Marks)

   (b) State Shannons expansion theorem and using this theorem expand the following expression

   $$f = \overline{b} + \overline{a}C$$ (4 Marks)

Contd.... 2

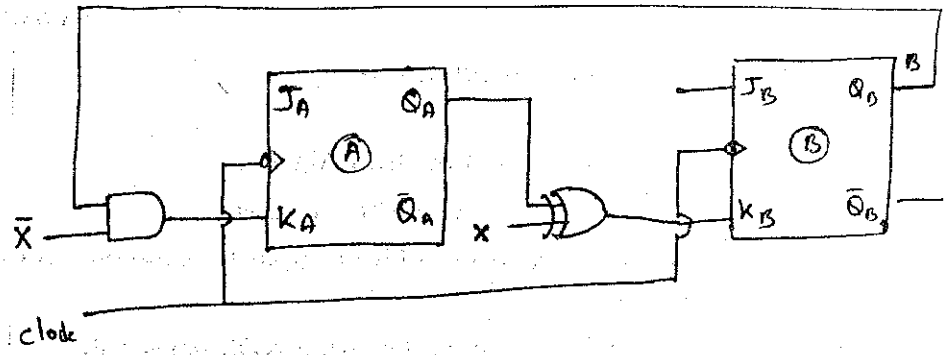
(c) Design a MOD - 4 synchronous down counter using JK flip flops and implement it. (8 Marks)

7. (a) Define and explain prime implicate. (5 Marks)

(b) Solve the following expression using Boolean algebra technique

$$F = \overline{\overline{A\overline{B} + A(\overline{\overline{A} + \overline{C}}) + \overline{A \oplus \overline{B}}}}$$ (5 Marks)

(c) Derive transition table. State table and state diagram for moore sequential circuit shown in below figure. (10 Marks)



8. (a) Explain the working of a CMOS, NOT, NAND and NOR gates. (8 Marks)

(b) Implement the following multi-Boolean function using PROM PLD

$f_1(x_1, x_0) = \overline{x_1} + x_0$
$f_2(x_1, x_0) = x_1$ (4 Marks)

(c) $f(a,b,c,d) = \sum m(1,2,3,5,6,7,11,12,13,14,15)$
for the above expression

i) Draw the logic diagram using AOI logic for minimal sum. Obtain minimal sum using K-map.

ii) Find all the prime implicants and essential prime implicants. (8 Marks)

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NEW SCHEME

CS33

USN | | | | | | | | | | |

Third Semester B.E. Degree Examination, January/February 2004

Common to BM/EC/EE/TE/ML/IT/CS/IS

Logic Design

Time: 3 hrs.] [Max.Marks : 100

Note: *1.Answer any FIVE full questions.*
2.All questions carry EQUAL marks.

1. (a) Explain the principle of duality. (4 Marks)
   (b) Mention two categories of Boolean expressions based on their structure. Write these forms for any give three - variable function $T(x, y, z)$. (8 Marks)
   (c) Give the Shanon's expansion theorem. (4 Marks)
   (d) Explain the exclusive-or-function. (4 Marks)

2. (a) Design an odd parity bit generator using gates for the decimal digits 0 to 9 represented in 84.21 BCD. Give the necessary truth table and draw the logic diagram. Explain. (8 Marks)
   (b) What code is used to label the row headings and column headings of a Karnaugh map and why? (4 Marks)
   (c) Using K-map obtain the minimal sum of products and the minimal product of sums form of the funciton $f(a, b, c, d) = \Sigma m(1, 2, 3, 5, 6, 7, 8, 13)$ (8 Marks)

3. (a) Mention one advantage and one disadvantage of the Quine-McCluskey method for obtaining the prime implicants of a given Boolean function. Obtain all the prime implicants of the function.
   $$f(v, w, x, y, z) = \Sigma m(4, 5, 9, 11, 12, 14, 15, 27, 30) + dc(1, 17, 25, 26, 31)$$
   Use Quinne-McCluskey method. Do you have any essential prime implicants. (12 Marks)
   (b) In what way MEV-K-map differs from the conventional K-maps? Simplify the function
   $$f(a, b, c, d) = \Sigma_m(2, 3, 4, 5, 13, 15) + dc(8, 9, 10, 11)$$
   using a two variable MEV-K-map. (8 Marks)

4. (a) With the aid of a neat circuit diagram explain the operation of a 2-input TTL nand gate with totem output. (8 Marks)
   (b) Discuss how a resistor could be constructed using MOSFET. Give the resistor characteristics. (6 Marks)
   (c) Draw the NMOS as well as PMOS circuit diagrams to realise a NAND gate. Give the relevant truth tables. (6 Marks)

5. (a) Explain a 4 bit parallel adder with the carry look ahead scheme. Clearly indicate how this scheme improves the performance of the operation. (10 Marks)
   (b) With the aid of block diagrams clearly distinguish between a decoder and encoder. (4 Marks)
   (c) Give a 4-to-1 MUX implementation of the three variable function
   $$f = \Sigma m(1, 4, 5, 7)$$
   (6 Marks)

Contd.... 2

6. (a) Write the logic diagram of a 4 bit bidirectional shift register with parallel load capability and briefly explain its operations. (10 Marks)

   (b) Explain Johnson counter with its circuit diagram, timing diagram and state diagram. (10 Marks)

7. (a) With the help of a neat block diagram, briefly discuss the CPU-memory connections. List the steps that takes place when the CPU

   i) Reads from memory ii) writes into memory. (10 Marks)

   (b) Explain the different types of read only memories. Give at least three applications of ROMs. (10 Marks)

8. Write short notes on :

   i) 4-bit magnitude comparator

   ii) Schmitt trigger

   iii) BCD adder

   iv) Flash memory (5×4=20 Marks)

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CSI—34

THIRD SEMESTER B.E. (COMPUTER SCIENCE AND ENGINEERING/ INFORMATION SCIENCE) DEGREE EXAMINATION, AUGUST/SEPTEMBER 2000

LOGIC DESIGN

Time : Three Hours Maximum : 100 Marks

Answer any **five** *questions.*

1. (a) Explain the Karnaugh map representation in detail and discuss the merits and demerits. (6 marks)

   (b) Give two simplified irredundant expressions for

   $$f(w, x, y, z) = \Sigma (0, 4, 5, 7, 8, 9, 13, 15).$$

   (14 marks)

2. (a) Explain the tabulation procedure in detail and discuss the merits and demerits. (6 marks)

   (b) Determine the set of prime implicants for the function

   $$f(w, x, y, z) = \Sigma (0, 1, 2, 5, 7, 8, 9, 10, 13, 15).$$

   (14 marks)

3. Design full-adder and full-subtractor. Give their truth tables, simplified expressions and circuit diagrams. (20 marks)

4. What is decoder ? What are its advantages ? Design a decimal decoder which converts information from BCD to decimal. (20 marks)

5. (a) Explain the operation of the SR flip-flop. (5 marks)

   (b) Explain the operation of the Master-Slave JK flip-flop along with its circuit diagram. (10 marks)

   (c) What is race-around condition ? Discuss in detail. (5 marks)

6. Design mode-3 counter using JK flip-flop. Sketch the waveforms for outputs when clock is applied and verify its operations. (20 marks)

7. (a) Explain four different types of read only memories. Give at least three applications. (15 marks)

   (b) Explain SRAM and DRAM. (5 marks)

8. Write short notes on the following :—

   (a) Shift registers.

   (b) Multiplexers.

   (c) Multivibrators.

   (d) PLA's. (20 marks)