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**Third Semester B.E. Degree Examination, May/June 2010**  
**Logic Design**

Time: 3 hrs.

Max. Marks:100

**Note: Answer any FIVE full questions, selecting  
at least TWO questions from each part.**

**PART – A**

- 1 a. Simplify the following expressions using k – map. Implement the simplified expression using basic gates :
  - i)  $T = f(wxyz) = \sum m(2, 3, 4, 5, 13, 15) + \sum d(8, 9, 10, 11)$
  - ii)  $R = f(abcd) = \pi M(2, 3, 4, 6, 7, 10, 11, 12).$  (12 Marks)
- b. Place the following equations into proper canonical form :
  - i)  $P = f(a, b, c) = ab' + ab' + bc$
  - ii)  $T = f(a, b, c) (a + b')(b' + c).$  (04 Marks)
- c. Define the following terms :
  - i) Minimum      iii) Canonical sum of products
  - ii) Maximum    iv) Canonical product of sum. (04 Marks)
- 2 a. Simplify the logic function given below using variable entered mapping (VEM) technique :  
 $f(a, b, c, d) = \sum m(2, 9, 10, 11, 13, 14, 15).$  (08 Marks)
- b. Simplify the following function using Quine-McClusky minimization technique :  
 $T = f(a, b, c, d) = \sum m(0, 1, 2, 3, 6, 7, 8, 9, 14, 15).$  (12 Marks)
- 3 a. Design a combinational logic circuit to output the 2's compliment of a 4-bit binary numbers:
  - i) Construct the truth table
  - ii) Simplify each output function using k-map and write reduced equations
  - iii) Draw the resulting logic diagram. (12 Marks)
- b. Construct a scheme to obtain a 4-to-16 line decoder using 74138 (3-8 line decoder). (05 Marks)
- c. Write a note on encodes. (03 Marks)
- 4 a. Realize the following Boolean function  $f(ABC) = \sum(0, 1, 3, 5, 7)$  using,
  - i) 8 : 1mux(74151)
  - ii) 4 : 1mux(74153). (06 Marks)
- b. Design a comparator to check if two n-bit numbers are equal. Configure this using cascaded stage of 1 bit equality comparator. (08 Marks)
- c. Implement full subtractor using gates and write a truth table. (06 Marks)

**PART – B**

- 5 a. Explain the operation of SR latch. Explain one of its applications. (12 Marks)
- b. Draw the logic diagrams for
  - i) Gated SR latch                      iii) Master slave JK flip flop
  - ii) Master slave SR flip flop        iv) Positive edge triggered 'D' flip flop. (08 Marks)
- 6 a. Differentiate between combinational logic circuit and sequential logic circuits. (03 Marks)
- b. Explain universal shift register with the help of logic diagram, mode control table and symbol. (09 Marks)
- c. Explain Jonsen counter, with its circuit diagram, and timing diagram. (08 Marks)

- 7 a. Explain Moore and Mealy models for clocked synchronous sequential circuits. (10 Marks)  
 b. Construct the excitation table, transition table, state table and state diagram, for the Moore sequential circuit shown in Fig. Q7(b). (10 Marks)

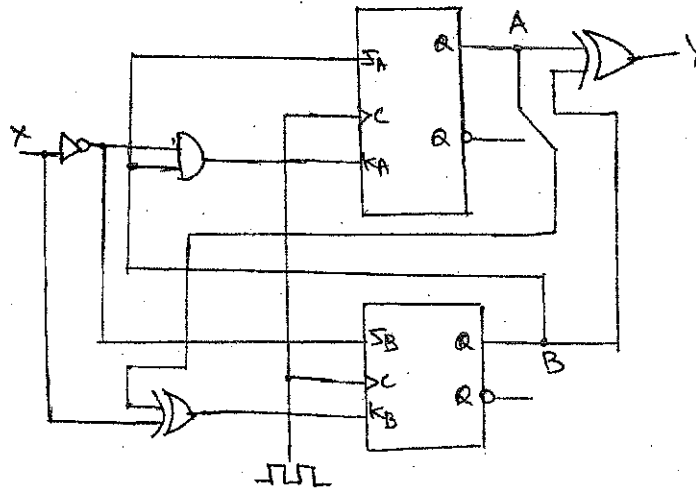


Fig. Q7(b)

- 8 a. Write a note on construction of state diagram. (05 Marks)  
 b. Design a counter using JK-flip flops whose counting sequence is 000, 001, 100, 110, 111, 101, 000 etc., by obtaining its minimal sum equations. (10 Marks)  
 c. Write a note on characteristic equations. (05 Marks)

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