

Third Semester B.E. Degree Examination, June / July 08
Logic Design

Time: 3 hrs.

Max. Marks:100

Note : Answer any FIVE questions, choosing atleast two from each part.

PART - A

- 1 a. Simplify the following expression using Karnaugh Map. Implement the simplified circuit using the gates as indicated.
- $f(ABCD) = \sum m(2,3,4,5,13,15) + \sum \alpha(8,9,10,11)$ use only NAND gates
 - $f(ABCD) = \pi(2,3,4,6,7,10,11,12)$ use only NOR gates
- to implement these circuits. (12 Marks)
- b. Fig shows a BCD counter that produces a 4-bit output representing the BCD code for the number of pulses that have been applied to the counter input. For example, after four pulses have occurred, the counter outputs are $(ABCD) = (0100)_2 = (04)_{10}$. The counter resets to 0000 on the tenth pulse and starts counting over again. Design the logic circuit that produces a HIGH output. Whenever the count is 2, 3 or 9. Use K-mapping and take advantages of "don't care" conditions. Implement the logic circuit using NAND gates.

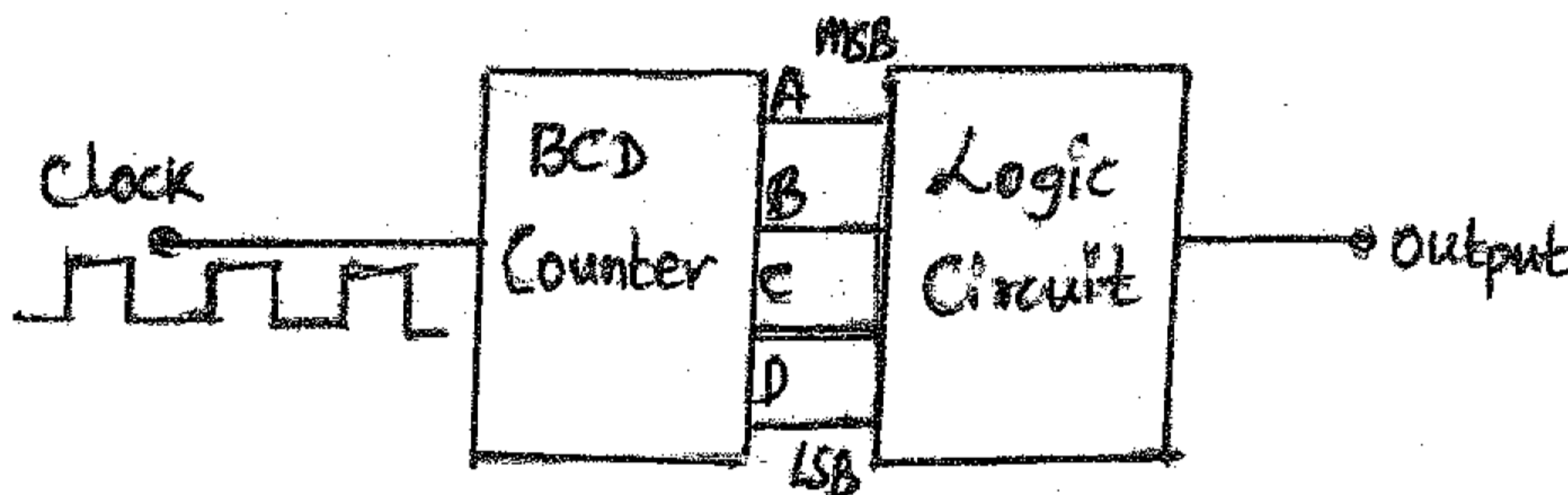


Fig. Q 1(b)

(08 Marks)

- 2 a. Simplify the logic function given below, using Quine-McCluskey minimization technique.
 $Y(ABCD) = \sum m(0,1,3,7,8,9,11,15)$. Realize the simplified expression using universal gates. (12 Marks)
- b. Simplify the logic function given below using variable - entered mapping (VEM) technique. $Y(ABCD) = \sum m(1,3,4,5,8,9,10,15) + \sum d(2,7,11,12,13)$. (08 Marks)
- 3 a. Realize the following Boolean function $f(ABCD) = \sum(0,1,3,5,7)$
Using – i) 8 : 1 MUX(74151) ii) 4 : 1 MIX(74153). (08 Marks)
- b. Design a combinational logic circuit that will convert a straight BCD digit to an Excess - 3 BCD digits.
- Construct the truth table
 - Simplify each output function using Karnaugh Map and write the reduced equations.
 - Draw the resulting logic diagram. (12 Marks)
- 4 a. Design a 4-bit BCD adder circuit, using 7483 IC chip, with self correcting circuit. i.e., a provision has to be made in the circuit, in case if the sum of the BCD number exceeds 9. (12 Marks)
- b. Design a combinational circuit that accepts two unsigned 2-bit binary number and provides 3 outputs.
Inputs : word $A = A_1A_0$, word $B = B_1B_0$.
Output : $A = B$, $A > B$, $A < B$. (08 Marks)

PART - B

- 5 a. Derive the characteristics equations of the following flip flops.
 i) SR flip flops ii) JK flip flop. (10 Marks)
 b. Explain clearly the operation of an asynchronous inputs in a flip flops with suitable example. (06 Marks)
 c. An edge triggered 'D' flip flop is connected as shown in the Fig. Q 5(b). Assume that $Q = 0$ initially and sketch the wave form and determine its frequency of the signal at 'Q' output.

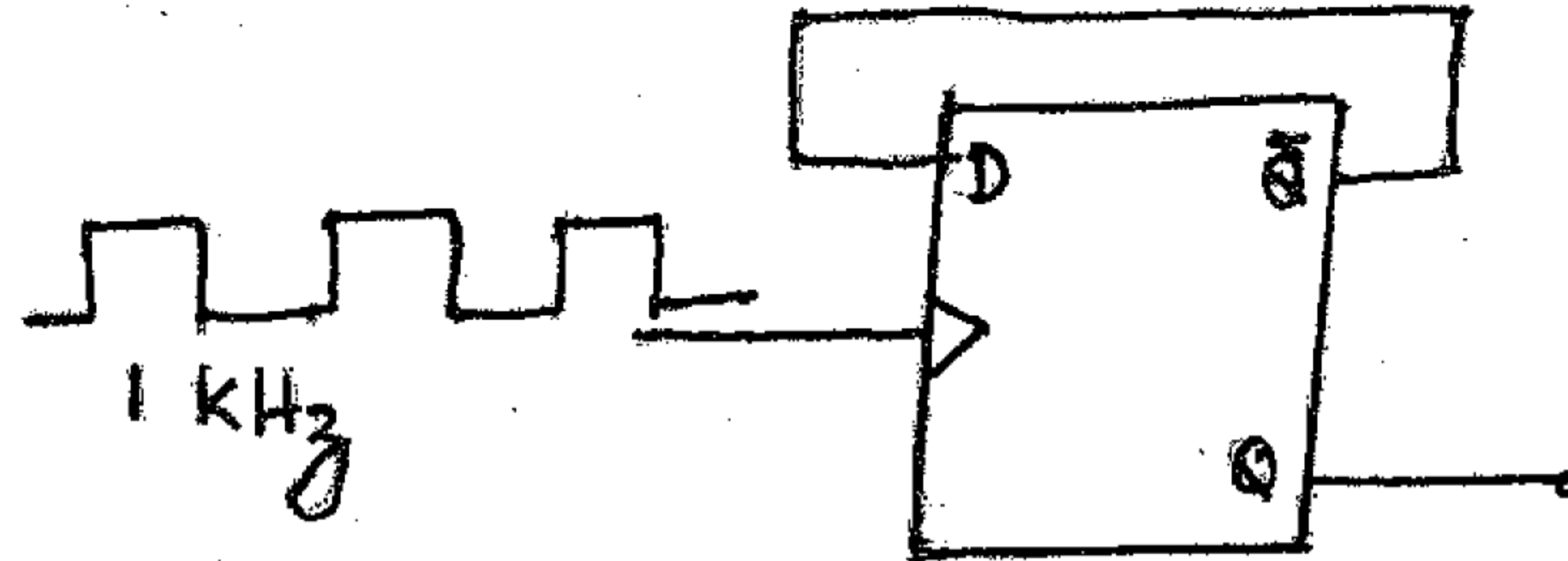


Fig. Q 5(C)

(04 Marks)

- 6 a. With the help of a suitable example, explain the following operations in a shift register.
 i) SISO ii) PISO iii) Twisted ring counter. (10 Marks)
 b. Design a ripple counter to count the following sequence, 1111, 1110, 1101, 1100, 1011, 1111, 1110, 1101, 1100, 1011, etc. Suggest a suitable circuit using 7490 and other gates to obtain the desired result. (10 Marks)
- 7 a. With a suitable example, explain the Mealy and Moore Model of a sequential circuit. (10 Marks)
 b. Construct the state table for the following state diagram.

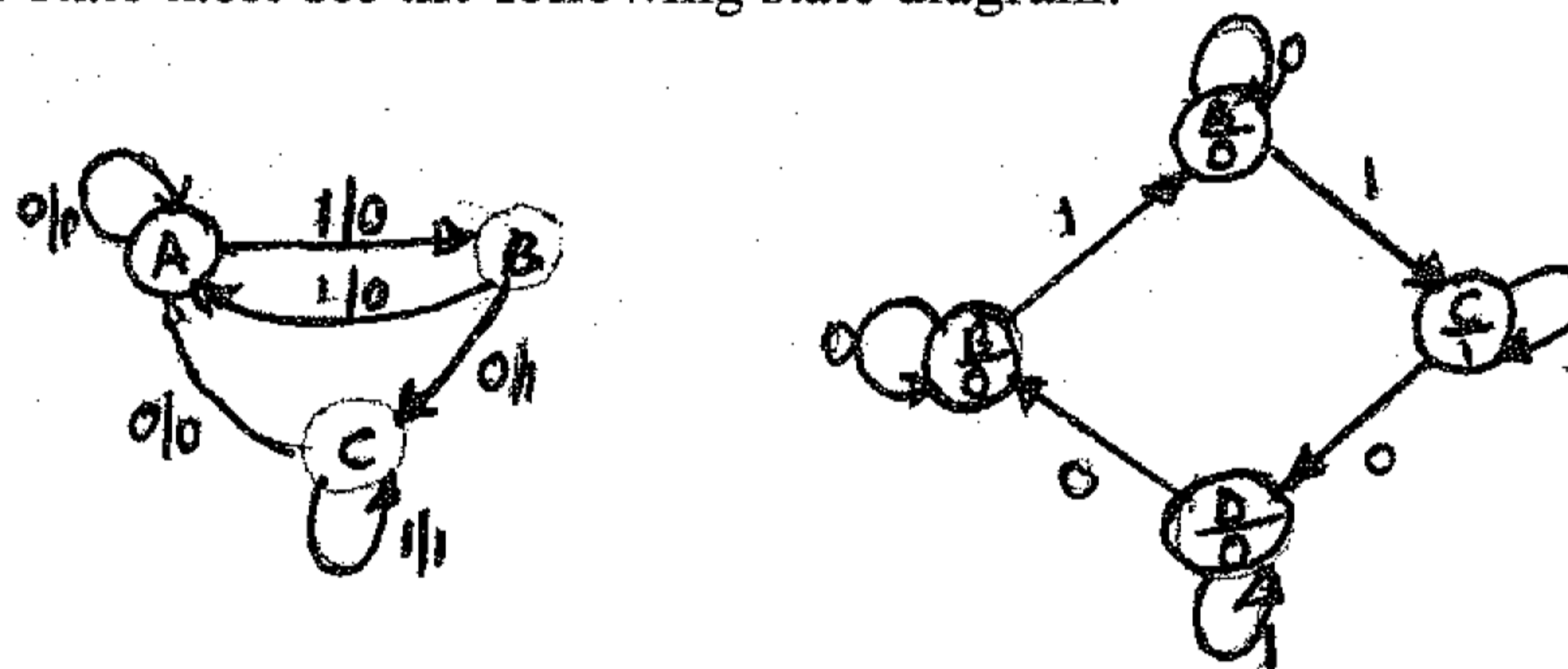


Fig. Q 7(c)

(10 Marks)

- 8 a. Design a clocked sequential circuit that operates according to the state diagram shown. Implement the circuit using D - flip flop.

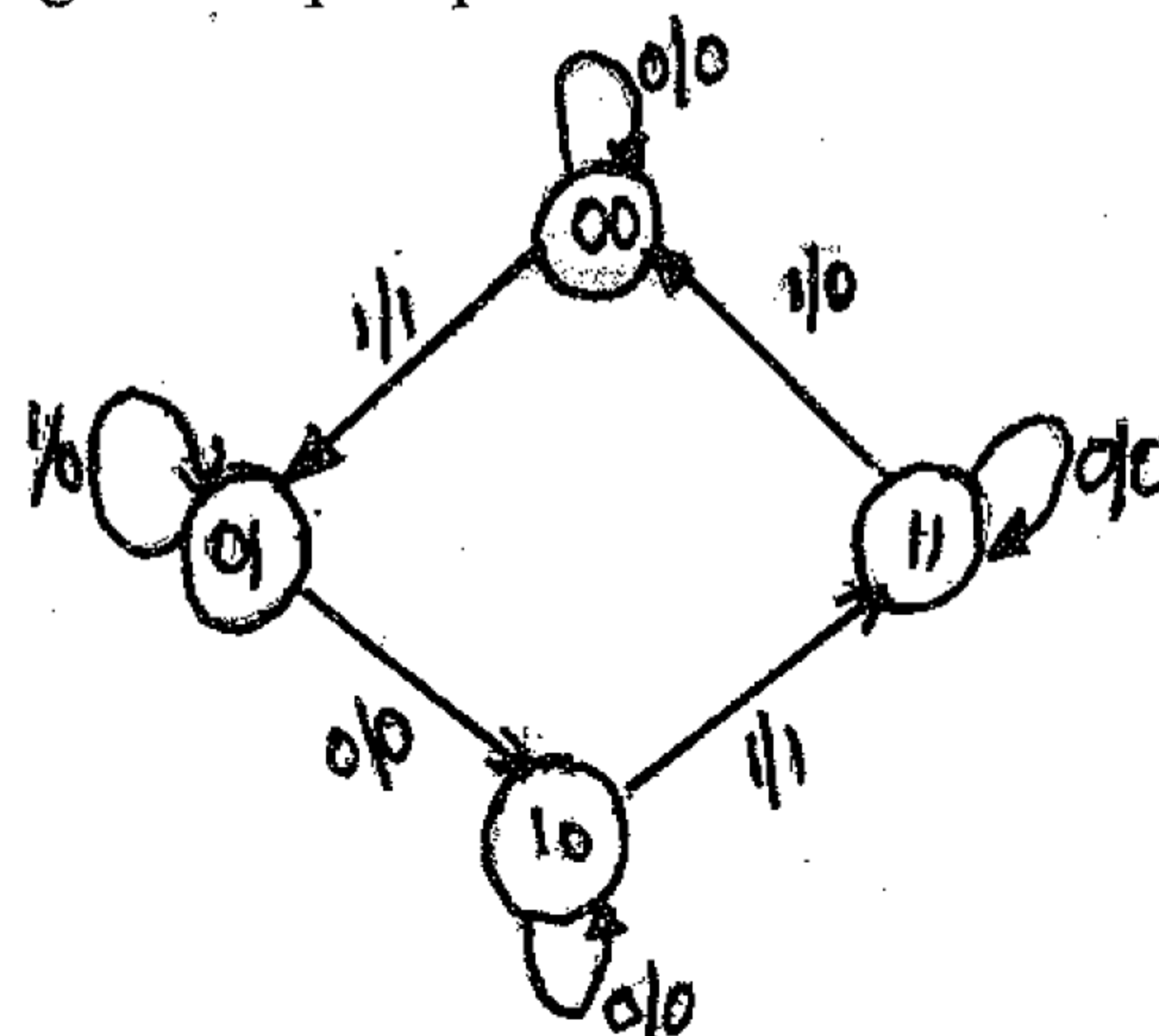


Fig. Q 8(a)

(12 Marks)

- b. Design a counter using JK - flip flops whose counting sequence is 000, 001, 100, 110, 111, 101, 000 etc. by obtaining its minimal sum equations. (08 Marks)
