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06ES32

Third Semester B.E. Degree Examination, June / July 08
Analog Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions, selecting atleast two questions from each part.***

PART A

1 a. Differentiate between static and dynamic resistance of a semi conductor diode. **(04 Marks)**

b. Explain with the help of a circuit diagram the working of a Full Wave Rectifier. Derive expressions for i) I_{dc} ii) I_{rms} iii) V_{dc} iv) Ripple factor v) Rectifier efficiency. **(10 Marks)**

c. For the circuit shown, in Fig.Q1(c) write the transfer characteristic equations. Assume diodes are ideal. Plot V_0 against V_i, indicating all slopes and voltage levels. **(06 Marks)**

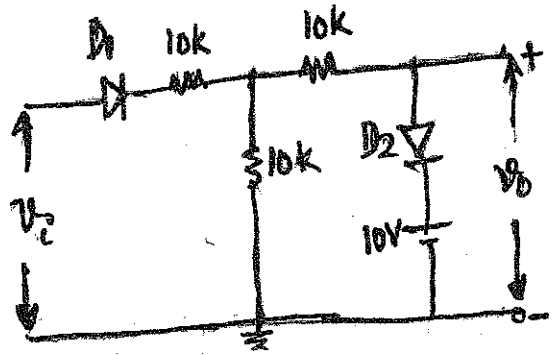

Fig.Q1(c)

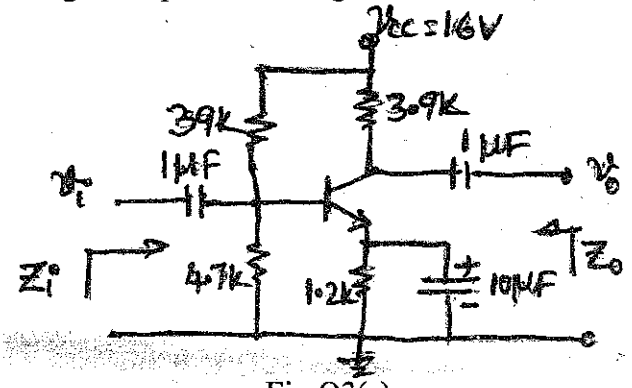

Fig.Q3(a)

2 a. Design a voltage divider bias circuit with V_{CC} = 10 V, R_C = 1.5 K ohm, I_C = 2 mA, V_{CE} = 5 V, β = 50. Assume silicon transistor and stability factor S = 5. **(08 Marks)**

b. Derive an expression for the stability factor $S(I_{CO})$ for a voltage divider bias circuit. **(08 Marks)**

c. Determine R_B and R_C for the transistor inverter of Fig.Q2(c) if I_{Csat} = 10 mA. **(04 Marks)**

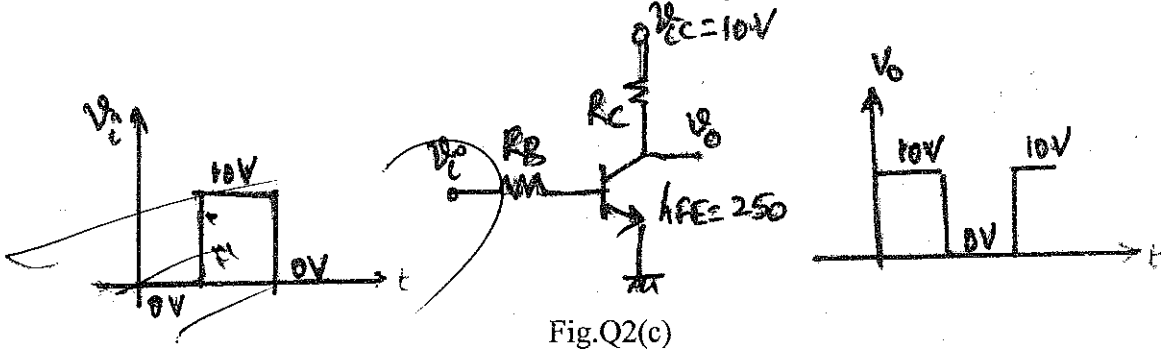

Fig.Q2(c)

3 a. For the network of Fig.Q3(a): i) Determine r_e ii) Calculate Z_i and Z_0 iii) Find A_V Given β = 100 S_i transistor. **(08 Marks)**

b. Draw the emitter follower circuit. Derive expressions for:
i) Z_i ii) Z_0 iii) A_V using r_e model. **(08 Marks)**

c. Define h-parameters. Draw the h-parameter model of a transistor. **(04 Marks)**

4 a. Determine the lower cutoff frequency for the network of Fig.Q4(a). Given β = 100, $r_0 = \infty$ ohm. Determine the mid band gain. If C_{be} = 36 pF, C_{bc} = 4 pF, C_{w_i} = 6 pF, C_{w_0} = 8 pF. Determine f_{H_i} and f_{H_0} and sketch the frequency response for low and high frequency regions using the results. **(12 Marks)**

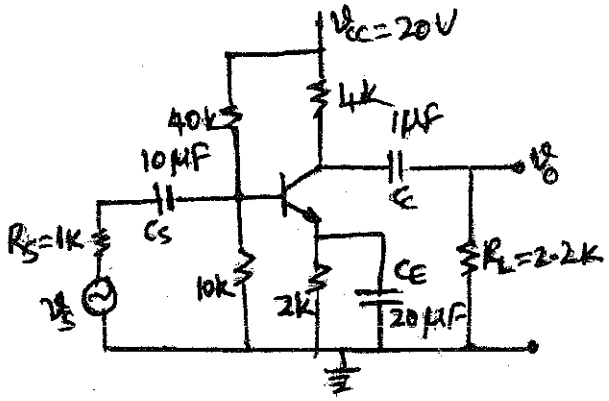

Fig.Q4(a)

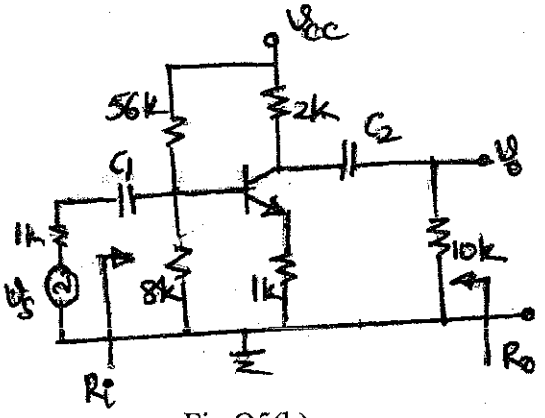

Fig.Q5(b)

b. Calculate the overall lower 3 db and upper 3 db frequencies for a 3 stage amplifier having an individual $f_1 = 40$ Hz and $f_2 = 2$ MHz. **(08 Marks)**

PART B

5 a. Draw the cascade configuration and list the advantages of this circuit. **(04 Marks)**

b. Determine A_i, R_i, A_v and R_0 for the circuit shown in fig.Q5(b). Given h parameters $h_{ie} = 1.1$ k ohm, $h_{re} = 2 \times 10^{-4}$, $h_{oe} = 25 \times 10^{-6}$ ℧, $h_{fe} = 50$. **(08 Marks)**

c. List the advantages of negative feedback amplifier. Derive expressions for Z_{if} and Z_{of} for voltage series feedback amplifier. **(08 Marks)**

6 a. Explain the working of a class B push pull amplifier. Prove that the maximum efficiency is 78.5%. **(10 Marks)**

b. A single transistor amplifier with transformer coupled load produces harmonic amplitudes in the output as $B_0 = 1.5$ mA, $B_1 = 120$ mA, $B_2 = 10$ mA, $B_3 = 4$ mA, $B_4 = 2$ mA, $B_5 = 1$ mA. i) Determine the percentage total harmonic distortion

ii) Assume second identical transistor is used along with suitable transformer to provide push pull operation. Using the above harmonic amplitudes, determine the new total harmonic distortion. **(10 Marks)**

7 a. Explain with the help of a circuit diagram, the working of an RC phase shift oscillator. **(08 Marks)**

b. With the help of Barkhousen criterion, explain the working of a BJT crystal oscillator. **(08 Marks)**

. Calculate the frequency of a Wien Bridge oscillator circuit when R = 12 k ohm and C = 2400 pf. **(04 Marks)**

8 a. Determine Z_i, Z_0 and A_v for the circuit shown in Fig.Q8(a), if $Y_{fs} = 3000$ μs and $Y_{os} = 50$ μs. **(06 Marks)**

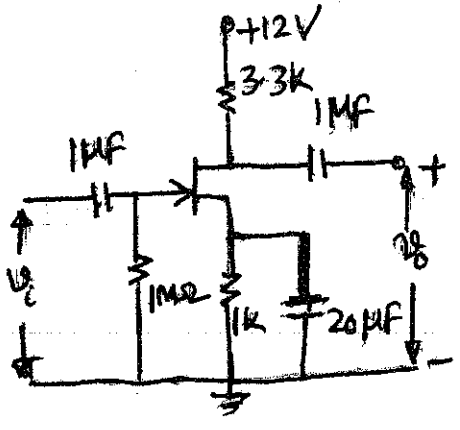

Fig.Q8(a)

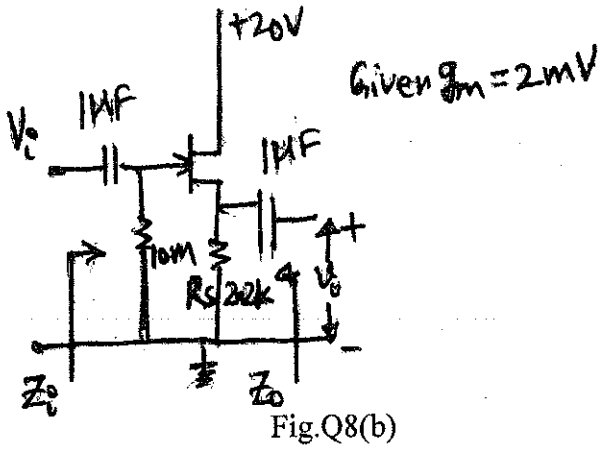

Fig.Q8(b)

b. Determine Z_i, Z_0, and A_v if $r_d = 40$ kΩ for fig.Q8(b). **(06 Marks)**

c. With the help of circuits and equations, show different biasing arrangements for depletion type MOSFET. **(08 Marks)**

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EC32

Third Semester B.E. Degree Examination, June / July 08
Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. For the sketch shown in fig.Q1(a) below, V_i varies from 0 to 150V. Sketch the output voltage V_o to the same time scale as the input voltage. Assume diodes to be ideal. **(08 Marks)**

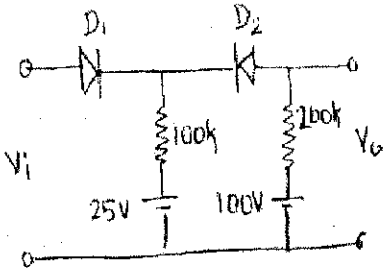

Fig. 1(a)

b. Explain the operation of full wave voltage doubler circuit. **(07 Marks)**

c. A full wave rectifier circuit is fed from a secondary center tapped transformer. The rms voltage from either end of secondary to center tap is 30V if diode resistance $R_f = 2\Omega$, half secondary resistance $R_S = 8\Omega$ and load $R_L = 1k\Omega$, calculate efficiency of rectification. **(05 Marks)**

2 a. Discuss the causes for bias instability in a transistor. **(05 Marks)**

b. With neat circuit diagram, explain how compensation for V_{BE} can be obtained using diode in emitter circuit of a transistor. **(05 Marks)**

c. A Ge transistor used in self biased circuit has $V_{CC} = 20V$, $R_C = 2k$, operating point $V_{CE} = 10V$ and $I_C = 4mA$, and $\beta = 50$. Calculate R_1, R_2 and R_E if stability factor $S = \delta I_C / \delta I_{CO} = 10$ is desired. **(10 Marks)**

3 a. Discuss the biasing techniques used for linear integrated circuits. **(08 Marks)**

b. Derive the expression for $A_V A_I R_{in}$ and R_o of an emitter follower. **(12 Marks)**

4 a. Derive the expression for transistor transconductance g_m and input conductance. $g_{b'c}$ in the case of transistor. **(12 Marks)**

b. State and prove Miller's theorem. **(08 Marks)**

5 a. Derive an expression for input and output resistance of voltage series feedback amplifier. **(12 Marks)**

b. An amplifier with negative feedback has a voltage gain of 120. It is found that without feedback, an input signal of 60mV is required to produce a particular output, where as with feedback the input signal must be 0.5V to get the same output. Find the Av and β of the amplifier. **(04 Marks)**

c. Mention the advantages of negative feedback. **(04 Marks)**

6 a. Derive an expression for the maximum conversion efficiency of a class B push – pull amplifier. **(10 Marks)**

b. Calculate the input power, output power and efficiency of the amplifier in the figure Q6(b) shown for an input voltage in a base current of 10mA peak. Also calculate the power dissipated by the transistor. **(10 Marks)**

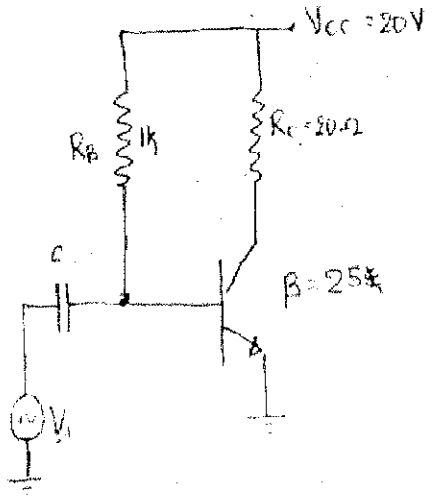

Fig.6(b)

7 a. Draw the circuit and explain how to measure the CMRR of an OP-amp. **(06 Marks)**

b. Find output voltage V_o in terms of V_1 and V_2 for the op-amp circuit shown in fig.7(b). Assume ideal op-amps. **(08 Marks)**

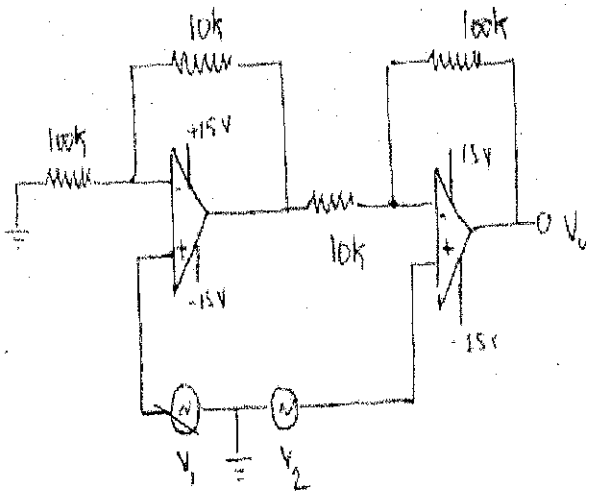

Fig. 7(b)

c. Design a Schmitt trigger whose V_{LT} and V_{UT} are $\pm 5V$. Draw waveforms. Take LM741 with $V_{sat} = \pm 13.5V$ and supply voltage $\pm 15V$. **(06 Marks)**

8 a. Draw and explain the working of positive clamper. **(06 Marks)**

b. Explain the working of D/A converter [Binary weighted resistors] with neat sketch. **(06 Marks)**

c. Give the circuit schematic off 555 timer connected as an astable multivibrator. Describe its operation. **(08 Marks)**

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06CS32

Third Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Sketch and explain the circuits of a combination clipper which limit the output between ± 10 V. Assume the diode voltage is 0.7 V. **(08 Marks)**

b. With neat diagram and waveforms explain the working of a negative clamper and also write the condition for stiff clamper. **(08 Marks)**

c. Explain how charge storage is overcome in Schottky diodes. **(04 Marks)**

2 a. Explain small signal operation of amplifiers **(06 Marks)**

b. What is the significance of ac emitter resistance in common emitter amplifier? **(04 Marks)**

c. Calculate the input impedance of the base in Fig. Q 2(c) with $\beta = 150$ also draw the ac equivalent circuit using π model. **(10 Marks)**

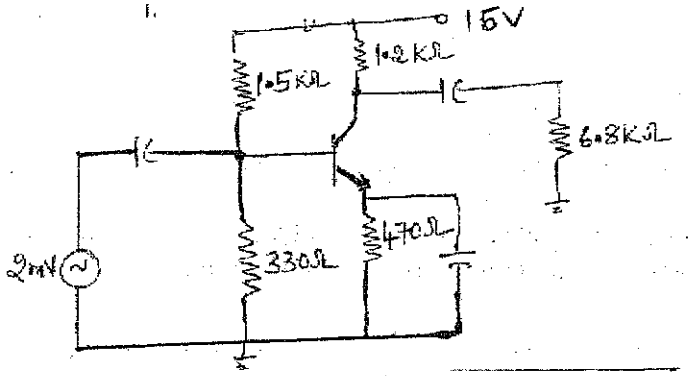

Fig. Q 2(c)

3 a. With a neat sketch explain the working of a swamped amplifier and derive the expressions for voltage gain and input impedance of the base. **(10 Marks)**

b. Calculate the output impedance of the amplifier in Fig. Q 3(b). **(06 Marks)**

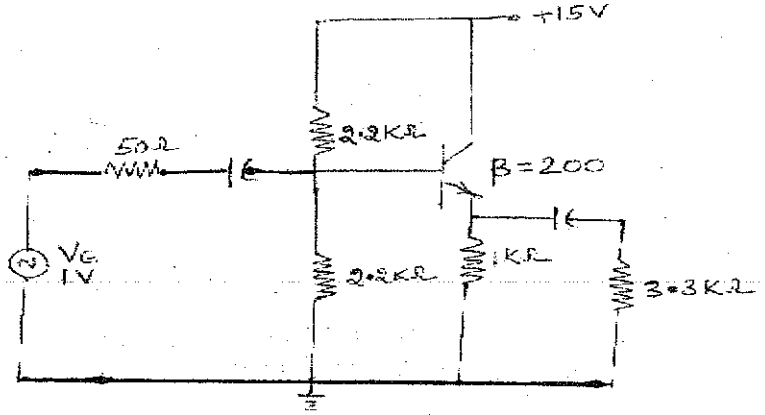

Fig. Q 3(b)

c. Write a note on complementary Darlington pair. **(04 Marks)**

4 a. Explain the working of class B push pull emitter follower. Draw its DC and AC load lines. **(10 Marks)**

b. Calculate the efficiency and transistor power dissipation of the class A amplifier shown in Fig. Q 4(b) if the peak to peak output voltage is 18 V and input impedance of the base is 100Ω.

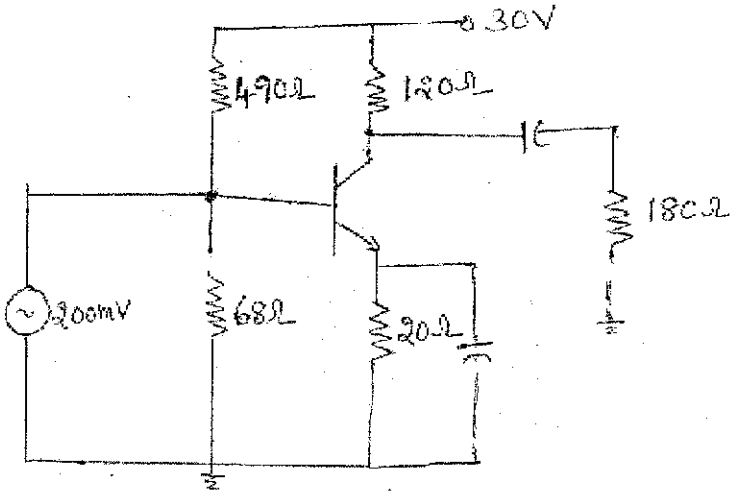

Fig. Q4(b) **(10 Marks)**

5 a. Describe the drain curves and Transconductance curve of enhancement mode MOSFET. **(08 Marks)**

b. Explain active load switching. How it advantages over passive load switching? **(06 Marks)**

c. With a neat circuit diagram explain CMOS inverter. **(06 Marks)**

6 a. Draw the frequency response of an AC amplifier. Define the terms cut off frequency, mid band gain. Derive the expression for gain in terms of mid band gain and cut off frequencies. **(06 Marks)**

b. OP Amp 74 IC has a mid band gain of 100,000, lower cut off frequency of 10 Hz and roll of rate 20 dB per decade. What is the voltage gain at 10 kHz? **(06 Marks)**

c. Explain ICVS amplifier. **(08 Marks)**

7 a. Design an OP Amp relaxation oscillator for a frequency of 1 kHz. Also draw the output waveform and waveform across the capacitor. **(10 Marks)**

b. Write the functional block diagram of IC 555 timer. Explain astable operation with the circuit diagram. Also draw the output waveform and waveform across the capacitor. **(10 Marks)**

8 a. Define load regulation, line regulation and output resistance for a voltage regulator. For a regulator the measured values are V_{NL} = 9.91 V, V_{FL} = 9.81 V, V_{HL} = 9.94 V and V_{LL} = 9.79 V. Calculate the load regulation and line regulation. **(10 Marks)**

b. What are switching regulators? Explain buck regulator. **(10 Marks)**

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06CS32

Third Semester B.E. Degree Examination, June / July 08
Electronic Circuits

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions, choosing atleast two questions from each part.***

PART - A

1 a. Explain the working of a negative clipper with its ct diagram. **(05 Marks)**

b. Sketch the wave form output V_{out} in the following circuit, indicating the values of maximum positive and negative output voltages.

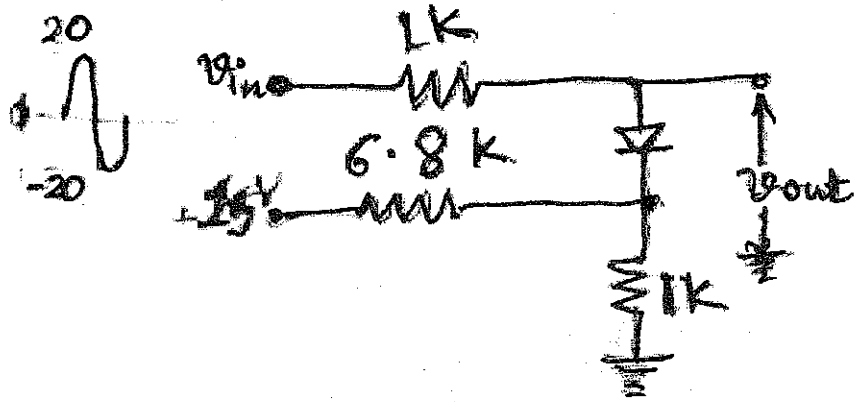

Fig. Q 1(b) **(05 Marks)**

c. Explain the working of a positive clamper with suitable diagrams. **(05 Marks)**

d. Explain the working of Schottkey diode. **(05 Marks)**

2 a. What is the ac collector voltage in the first stage of the amplifier circuit shown in Fig. Q 2(a)? Calculate the output voltage V_{out} across the load resistor.

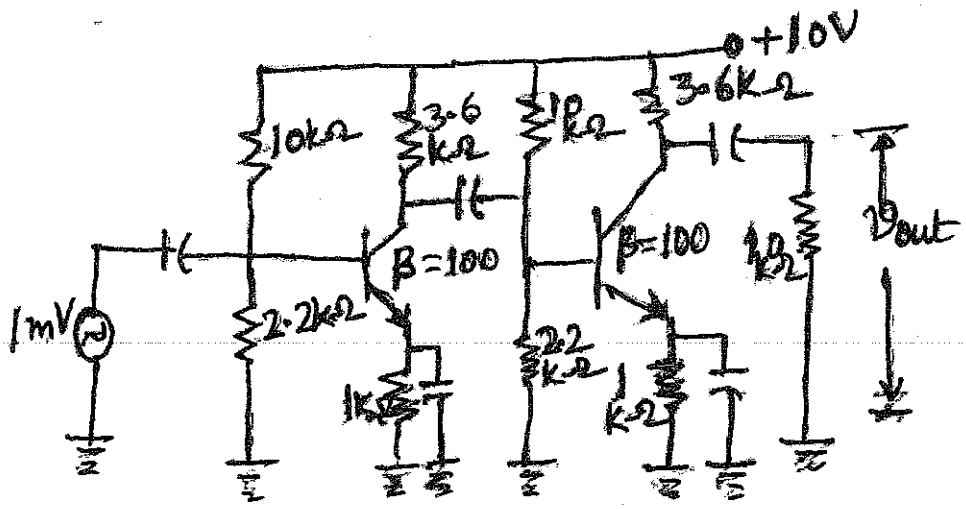

Fig. Q 2(a) **(10 Marks)**

b. Draw the circuit diagram of a swamped amplifier. Write down its ac equivalent circuit and derive expressions for Zin (base) and voltage gain A_v. **(10 Marks)**

3 a. With the help of a circuit diagram, explain the working of a voltage divider biased (VDB) amplifier, highlighting on bias stabilization. **(08 Marks)**

b. In the following circuit, what is the value of capacitor 'C' needed to efficiently short the point E to ground, if the input frequency is 1 kHz?

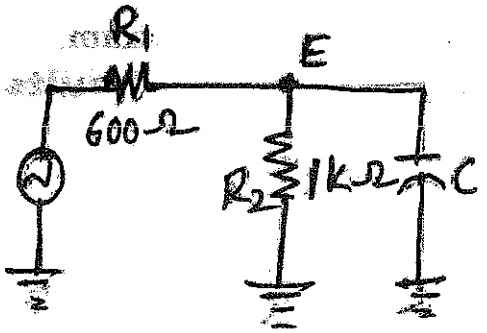

Fig. Q 3(b) **(06 Marks)**

c. Write down the circuit diagram of a base – biased amplifier and its ac equivalent circuit replacing the transistor by its π model. **(06 Marks)**

4 a. Explain the working of an emitter follower circuit with its circuit diagram and its ac equivalent circuit. **(06 Marks)**

b. Distinguish between class A, class B, class AB and class C amplifier. **(04 Marks)**

c. Calculate the voltage gain and the ac voltage of the following emitter follower if β = 150.

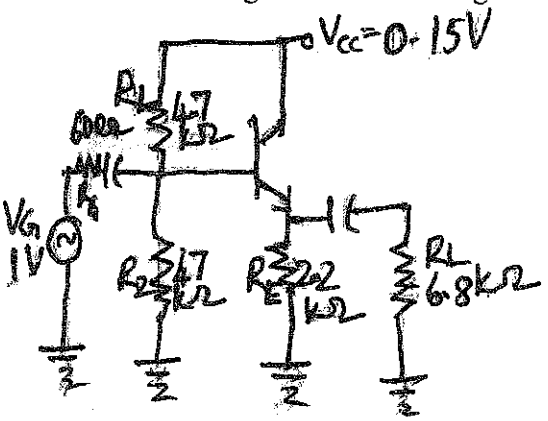

Fig. Q 4(c) **(10 Marks)**

PART - B

5 a. Explain the structure of the depletion mode MOSFET. And the D – MOSFET curves. **(10 Marks)**

b. Explain the active load switching circuit using the MOSFET. Draw its equivalent circuit and its two terminal curves. **(10 Marks)**

6 a. Explain the frequency response of an amplifier. Describe the effect of the components that reduces the response of the amplifier below and above the midband. **(08 Marks)**

b. Explain the four types of negative feed back amplifiers. **(12 Marks)**

7 a. Draw the circuit diagram of an integrator and explain its operation with a typical input pulse. **(10 Marks)**

b. Draw and explain the circuit diagram of voltage controlled oscillator using the 555 timer. **(10 Marks)**

8 a. Define the terms 'Load Regulation' and 'Line Regulation' with respect to a power supply. **(06 Marks)**

b. Describe with circuit diagram, the operation of a shunt regulation power supply.

c. What are the advantages and disadvantages of shunt regulator? What are the advantages of a series regulator? **(10 Marks)**

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EC32

Third Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Electronic Circuits

ime: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

a. Discuss voltage doubler circuit. **(05 Marks)**

b. Define regulation and derive equation for a fullwave circuit. **(07 Marks)**

c. In the Fig.1(c) the diodes are ideal. Write the transfer characteristic equations (V_o V_s V_i). Plot V_o V_s V_i . Indicate all intercepts, slopes and voltage levels.

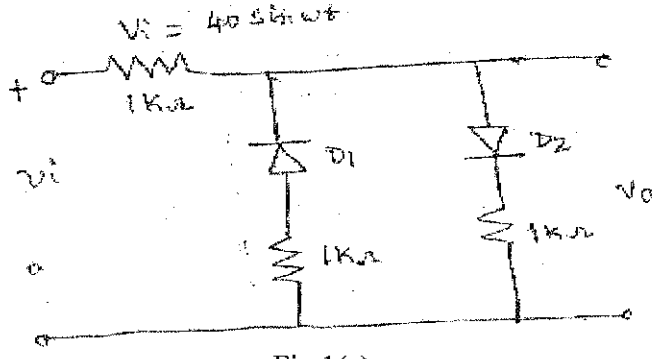

Fig.1(c)

Repeat for the case when $V_r = 1$ V $V_i = 40 \sin \omega t$ **(08 Marks)**

a. Define three stability factors. For a self bias circuit derive the expression for S_v and S_I. **(10 Marks)**

b. For the circuit shown in Fig.2(b) $V_{cc} = 24$ V, $R_c = 10$ kΩ, $R_e = 270$ Ω, $\beta = 45$. Silicon transistor is used under operationing condition $V_{ce} = 5$V find

i) R ii) Stability factor S

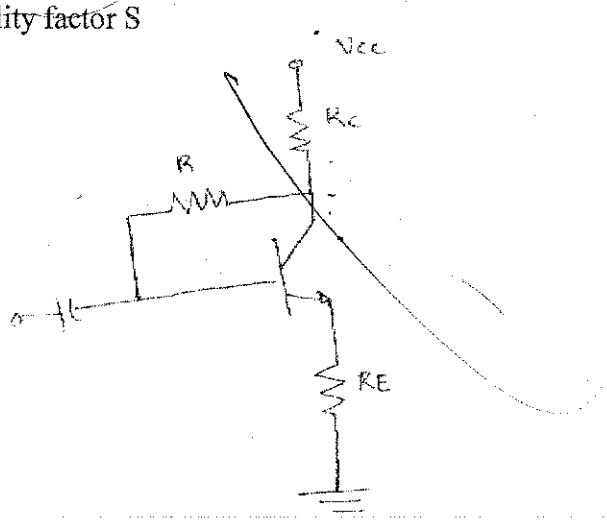

Fig.2(b) **(06 Marks)**

c. Briefly discuss how do you provide operating point stability using compensation technique. **(04 Marks)**

a. Using small signal low frequency hybrid model for the CE amplifier with a load of Z_L and source resistance R_S derive expression for A_I, A_V, Z_i and Z_o. **(10 Marks)**

b. For a transistor amplifier in CB configuration find A_I, A_V, Z_{in}, Z_{out}, A_{VS} and A_{IS} given that $h_{ib} = 22\ \Omega$, $h_{rb} = 2.9 \times 10^{-4}$, $h_{fb} = -0.98$, $1/h_ob = 2.04$ mΩ. **(06 Marks)**

c. State and Prove Miller's theorem. **(04 Marks)**

4 a. Draw small signal high frequency CE model for transistor and explain the significance of even component in the model and prove that $h_{fe} = g_m r_{b'e}$. **(08 Marks)**

b. Discuss the various types of distortion in amplifier. **(06 Marks)**

c. With suitable RC circuit calculate low frequency response of an amplifier. **(06 Marks)**

5 a. Explain the advantages of negative feed back circuit. **(06 Marks)**

b. Draw and explain different feed back amplifier topologies. **(08 Marks)**

c. An amplifier with open loop voltage gain $A_V = 1000 \pm 100$ is available. It is necessary to have an amplifier whose voltage gain varies by no more than $\pm 0.1\%$.

i) Find the reverse transmission factor β of the feed back network

ii) Find gain with feedback. **(06 Marks)**

6 a. Show that the maximum conversion efficiency of class-B push pull amplifier is 78.5%. **(06 Marks)**

b. Discuss why even harmonics are not present in push-pull amplifier. **(06 Marks)**

c. Explain :

i) Input bias current compensation in OPAMP.

ii) Input offset voltage compensation for inverting and non inverting configuration. **(08 Marks)**

7 a. Design a single pole LPF with a cut off frequency of 10 kHz and mid band gain of 1.5. Draw the circuit diagram. **(05 Marks)**

b. With a neat diagram and relevant waveforms explain the following OPAMP circuits :

i) Peak detector and clamper

ii) Schmitt trigger

iii) Instrumentation amplifier **(10 Marks)**

c. Explain sample and hold act. **(05 Marks)**

8 a. With a neat diagram and relevant waveforms, explain the working of an astable modulator circuit using 555 timer. Obtain the expression for the time period. **(12 Marks)**

b. Discuss the specifications of a DAC circuit. **(08 Marks)**

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OLD SCHEME

Third Semester B.E. Degree Examination, July 2007
Electronics Circuits

Time: 3 hrs.] [Max. Marks:100

Note : ***1. Answer any FIVE full questions.***
2. Assume missing data suitably.

1 a. What is synchronization? With a neat circuit diagram and waveform explain the working of a UJT time base generator. **(10 Marks)**

b. Derive an expression for the junction current of a semiconductor diode. **(10 Marks)**

2 a. Draw the circuit diagram of a full wave bridge rectifier with capacitor filter and explain its operation with wave forms. **(10 Marks)**

b. Show that the maximum rectification efficiency of a fullwave rectifier is 81.2%. **(10 Marks)**

3 a. Sketch the CE I/O characteristics for a Si n-p-n BJT. Indicate the various regions of operation. Explain the shapes of the curves. **(10 Marks)**

b. Given $\beta = 50$ for the transistor circuit shown in Fig.3(b), find the transistor currents I_C, I_E and I_B. In which region is the transistor operating? Justify.

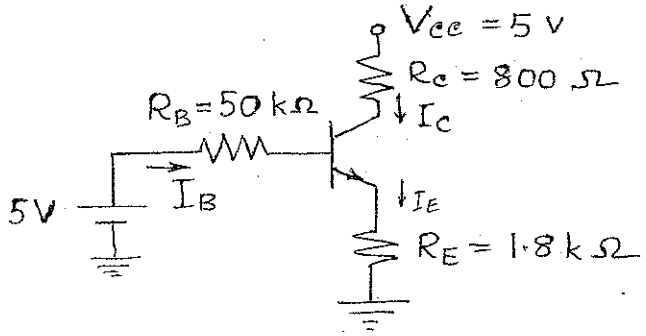

Fig.3(b) **(10 Marks)**

4 a. Derive expression for current gain, voltage gain and input impedance of a Darlington pair emitter follower. **(10 Marks)**

b. Compare different methods of couplings used in amplifiers with application. **(10 Marks)**

5 a. Write the hybrid-π model of BJT and briefly explain the various parameters of the model. **(08 Marks)**

b. Draw the circuit of a bootstrapped emitter follower and explain how it gives higher input impedance than emitter follower. **(08 Marks)**

c. The cutoff frequencies of a transistor amplifier are $f_1 = 500$ Hz and $f_2 = 400$ kHz. The midband voltage gain is 80. Find the voltage gain at 250 Hz. **(04 Marks)**

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6 a. For the emitter follower network of Fig.6(a), determine :
i) r_e ii) Z_i iii) Z_o iv) A_v v) A_i

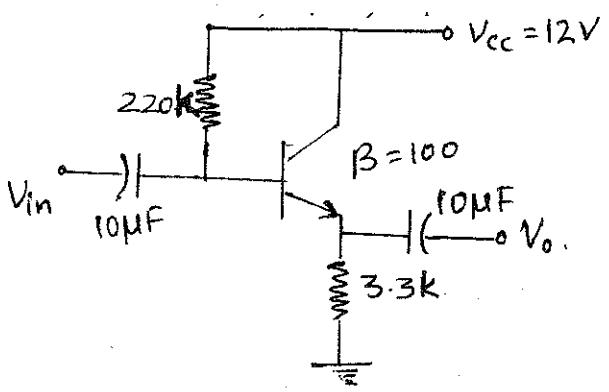

Fig.6(a)

Also derive the equations for Z_i, Z_o, A_v and A_i **(12 Marks)**

b. Explain with relevant sketches how power amplifiers are classified. Derive the expression for the conversion efficiency of a class B push pull amplifier. **(08 Marks)**

7 a. Show that the maximum conversion efficiency of a transformer coupled class A power amplifier is 0.5. **(08 Marks)**

b. In a class A transformer coupled power amplifier V_{CC} = 12 V, R_L = 1 kΩ, efficiency of a transformer is 75%. Power delivered to load is 1 Watt.
Find :
i) Turns ratio of transistor.
ii) Collector dissipation.
iii) D.C. power drawn from supply. **(06 Marks)**

c. What is cross over distortion and how is it minimized? **(06 Marks)**

8 Write short notes on :
a. Varactor diode.
b. Clipping circuits.
c. Shunt voltage regulator.
d. Significance of operating point in a transistor. **(20 Marks)**

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EC32

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NEW SCHEME

Third Semester B.E. Degree Examination, July 2007
EC/TE/EE/BM/ML/IT/CS/IS
Electronic Circuits

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Define diffusion capacitance. Derive an expression for the same. **(05 Marks)**

b. Draw the piece wise linear V-I characteristics of a P-N junction diode. Give the circuit model for the ON state and OFF state. **(05 Marks)**

c. The input voltage V_i to the two-level clipper circuit as shown in fig.1(c) varies linearly from 0 to 150 V. Sketch the output voltage V_0 to the time scale. Assume diodes as ideal. **(10 Marks)**

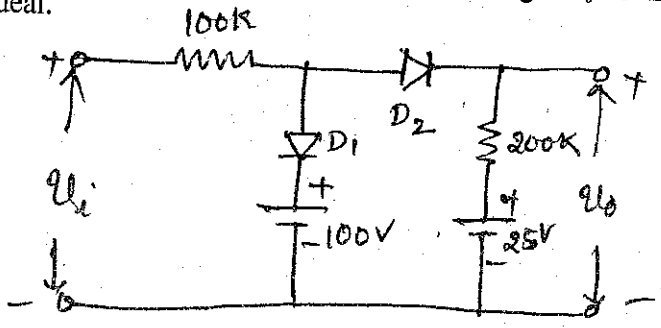

Fig.1(c)

2 a. With necessary circuit and waveforms, explain a bridge rectifier circuit with capacitor filter. Derive an expression for the ripple factor. **(10 Marks)**

b. Design a full wave rectifier filter to meet the following requirements. DC output voltage = 15 V, load resistance = 1 K, rms ripple voltage on capacitor <1 % of dc output voltage. The AC supply voltage is 230 V at 50 Hz. **(10 Marks)**

3 a. What is the need for bias compensation? Explain the compensation techniques used for V_{BE} and I_{CBO}. **(10 Marks)**

b. The circuit shown in fig.3(b) uses silicon transistor with $\beta = 45$, $V_{CC} = 24$ V, $R_C = 10$ K, R = 10 K, $R_E = 0.27$ K. If $V_{CE} = 5$ V under quiescent conditions, find the value of 'R' and the stability factor $S(I_{CO})$. **(06 Marks)**

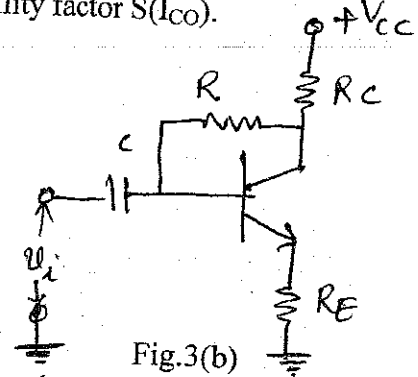

Fig.3(b)

c. What do you mean by thermal runway of a transistor? Explain. **(04 Marks)**

Contd.... 2

4 a. Obtain an expression in terms of 'h' parameters for a transistor as a two-port network. Using the above developed equations obtain the hybrid model of CE, CC and CB configurations. **(08 Marks)**

b. State and explain Millers theorem. **(04 Marks)**

c. A transistor is connected as a common emitter amplifier driving a load of 10 kΩ. It is supplied by a source of 1 kΩ internal resistance. The 'h' parameters are h_{ie} = 1.1 kΩ, h_{fe} = 50, h_{re} = 2.5 X 10^{-4}, $h_{oe} = \frac{1}{40\,k\Omega}$. Find: i) Current gain ii) Voltage gain iii) Input impedance iv) Output impedance. **(08 Marks)**

5 a. Derive an expression for: i) Input conductance ($g_{b'e}$) ii) Output conductance (g_{cc}) for a transistor at high frequency. **(06 Marks)**

b. Give the classification of multistage amplifier. Explain the various distortions in amplifiers. **(08 Marks)**

c. Discuss the general characteristics of a negative feedback amplifier. **(06 Marks)**

6 a. Derive an expression for input and output resistance of a voltage shunt feedback amplifier. **(06 Marks)**

b. Explain the different types of power amplifiers. **(08 Marks)**

c. An ideal class B- pushpull amplifier with input and output transformers, has V_{CC} = 20 V, $N_2 = 2N_1$ and R_L = 10 Ω. The transistors have h_{FE} = 20. Let the input be sinusoidal. For the maximum output signal $V_m = V_{cc}$. Determine: i) The output signal power ii) Collector power dissipation iii) Conversion efficiency. **(06 Marks)**

7 a. Obtain an expression for the closed loop gain of a non-inverting amplifier. **(07 Marks)**

b. With necessary sketch and characteristic curves explain the operation of a Schmitt trigger. **(08 Marks)**

c. What do you mean by precision rectifiers? Explain full wave precision rectifier. **(05 Marks)**

8 a. Explain the working of SAR ADC. **(06 Marks)**

b. Explain the working R - 2R ladder DAC. **(07 Marks)**

c. Explain the applications of astable multivibrator as:
i) Square wave generator ii) To achieve variable duty cycle control. **(07 Marks)**

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EC/TE/ML304

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OLD SCHEME

Third Semester B.E. Degree Examination, Dec. 06 / Jan. 07
EC / TE / ML
Electronics Circuits

Time: 3 hrs.] [Max. Marks:100

Note : ***1. Answer any FIVE full questions.***
2. Assume missing data suitably.

1 a. With a neat diagram explain the constructional feature of CRT and also explain the focusing scheme used in it. **(10 Marks)**
b. Derive an equation for diffusion capacitance of P-N junction diode. **(06 Marks)**
c. Distinguish between ideal and practical diodes. Draw piece-wire linear characteristic and explain. **(04 Marks)**

2 a. Draw the circuit diagram of a Bridge rectifier with capacitor filter and also derive the expression for ripple factor and rectifier efficiency. **(10 Marks)**
b. Explain the working of a double ended clipper using ideal diodes. Give its transfer characteristics. **(06 Marks)**
c. Explain the tunneling phenomenon in tunnel diodes. Draw its V-I characteristics **(04 Marks)**

3 a. Discuss the causes for bias instability in a transistor. **(06 Marks)**
b. Derive an equation for the stability factor S for a C.E. self bias circuit. **(08 Marks)**
c. Discuss different types of bias compensation technique used in the transistor circuits. **(06 Marks)**

4 a. Using approximate h-parameter model for the transistor, obtain expressions for Z_i, Z_0, A_v, A_I for a C.E self bias amplifier with unbypassed R_E. **(12 Marks)**
b. For the circuit shown in the Fig. 4(b) find, R_C, R_B, R_E, V_{CE} and V_B

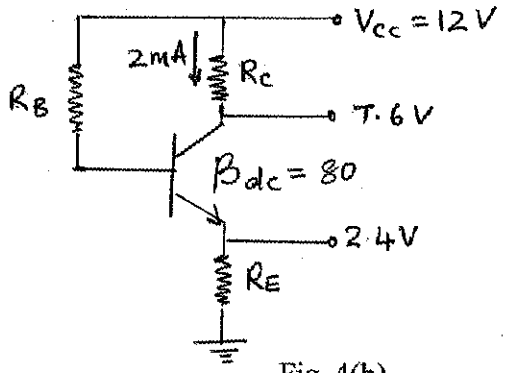

Fig. 4(b) **(08 Marks)**

5 a. Write the hybrid-π model of BJT and briefly explain the various parameters of the model. **(08 Marks)**
b. Draw the circuit of a bootstrapped emitter follower and explain how it gives higher input impedance than emitter follower.
c. The cutoff frequencies of a transistor amplifier are $f_1 = 500$ Hz and $f_2 = 400$ kHz. The midband voltage gain is 80. Find the voltage gain at 250 Hz. **(04 Marks)**

Contd.... 2

6 a. For the emitter follower network of Fig. 6(a), determine :
i) r_e ii) Z_i iii) Z_o iv) A_v v) A_i

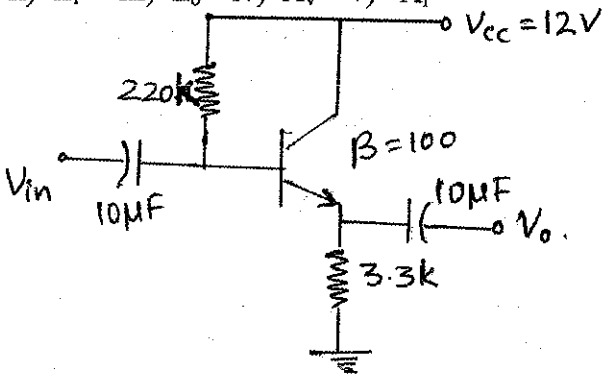

Fig. 6(a) **(12 Marks)**

Also derive the equations for Z_i, Z_o, A_v and A_i

b. Explain with relevant sketches how power amplifiers are classified. Derive the expression for the conversion efficiency of a class B push pull amplifier. **(08 Marks)**

7 a. With the circuit diagram explain the working principle of a shunt and series voltage regulator. Also obtain the expression for the regulated output voltage. **(12 Marks)**

b. What is switching regulator? Explain step-down type of switching regulator with a neat block diagram. **(08 Marks)**

8 Write short notes on the following :

a. Photo diodes
b. Ebbers Mol model of PNP transistor
c. Voltage doublers
d. Class A power amplifier. **(20 Marks)**

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EC32

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NEW SCHEME

Third Semester B.E. Degree Examination, Dec. 06 / Jan. 07
EE / EC / IT / TC / BM / ML / CS / IS
Electronics Circuits

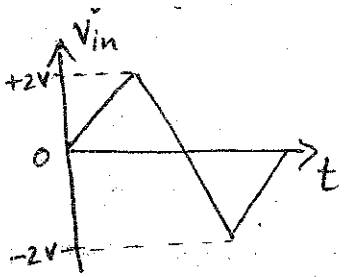
Time: 3 hrs.] [Max. Marks:100

Note : ***1. Answer any FIVE full questions.***
2. Missing data may be suitably assumed.

1 a. Explain diffusion capacitance. Obtain an expression for the diffusion capacitance in a P-N diode. **(07 Marks)**

b. What is a voltage multiplier circuit? Explain the operation of a full wave voltage doubler circuit. **(07 Marks)**

c. Assuming ideal diode in the circuit shown below, draw the output voltage for the given input signal.



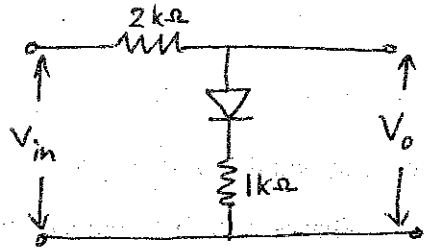


Fig.1(c) **(06 Marks)**

2 a. Draw and explain a double diode clipper circuit, which limits the output at two independent levels. **(06 Marks)**

b. Explain how a diode can be used in a transistor to compensate for changes in I_{CO}. **(06 Marks)**

c. For the circuit shown in the Fig.2(c) determine I_C, V_{CE}, R_1, V_B.

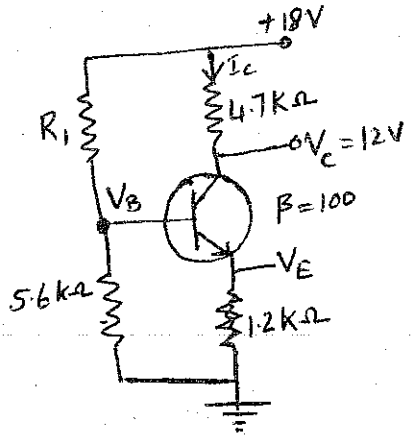


Fig.2(c) **(08 Marks)**

3 a. Explain how h-parameters can be obtained from the static characteristics of a transistor. **(06 Marks)**

b. State and explain Millers theorem. **(04 Marks)**

Contd.... 2

c. For the common emitter amplifier with collector to base bias shown in the Fig.3(c) Calculate : A_i, R_i, R_i', A_V and A_{VS}
Given : $h_{ie} = 1.1$ k ; $h_{fl} = 50$ $h_{oe} = 25\ \mu A/V$; $h_{re} = 2.5\times10^{-4}$

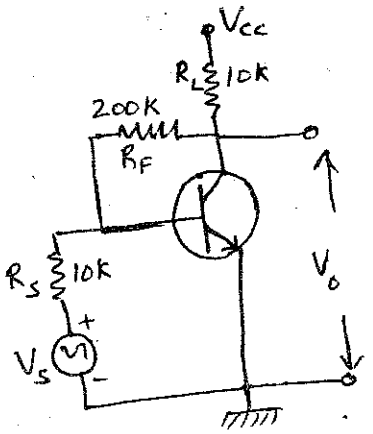


Fig.3(c) **(10 Marks)**

4 a. Draw the hybrid - π model of a transistor and explain the significance of each component in the model. **(06 Marks)**
b. Derive expressions for transistor transconductance g_m and input conductance $g_{b'e}$. **(10 Marks)**
c. Explain the various types of distortions encountered in amplifiers. **(04 Marks)**

5 a. What is negative feedback in amplifiers? Show that negative feedback increases the bandwidth of an amplifier. **(08 Marks)**
b. Derive an expression for the input resistance with feedback amplifier employing voltage series feedback. **(06 Marks)**
c. An amplifier with negative feedback has voltage gain 120. It is found that without feedback an input signal of 60mV is required to produce a particular output, whereas with feedback the input signal must be 0.5V to get the same input. Find A_V and β of the amplifier. **(06 Marks)**

6 a. Show that a transformer coupled class-A amplifier has a maximum power efficiency of 50%. **(07 Marks)**
b. With circuit diagram explain the working of class-B push-pull amplifier. Also obtain an expression for the maximum conversion efficiency of this amplifier. **(09 Marks)**
c. How much maximum power can be dissipated in the individual transistors of a class-B push-pull power amplifier if $V_{CC} = 20V$ and $R_L = 4\Omega$. **(04 Marks)**

7 a. With usual notations derive an expression for the voltage gain of a practical inverting op-amp. **(06 Marks)**
b. Describe a method of measuring and calculating CMRR of an op-amp. **(06 Marks)**
c. What are the advantages of active filters over passive ones? Design a first order high pass filter at a cutoff frequency of 10 kHz with a pass band gain of 1.5. **(08 Marks)**

8 a. Draw an inverting op-amp Schmitt trigger circuit and explain its working. **(06 Marks)**
b. Explain the principle of operation of a R-2R ladder type D to A converter. **(06 Marks)**
c. With the help of a neat diagram and relevant waveforms explain the working of a monostable multivibrator circuit using 555 timer. **(08 Marks)**

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EC-32

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NEW SCHEME

Third Semester B.E. Degree Examination, July 2006
Electronics and Communication
Electronic Circuits

Time : 3 hrs.] [Max. Marks : 100

Note : *1. Answer any FIVE full questions.*

1 a. Analyse the clipper circuit of Fig 1(a) and draw its output waveform and transfer characteristic curve. **(05 Marks)**

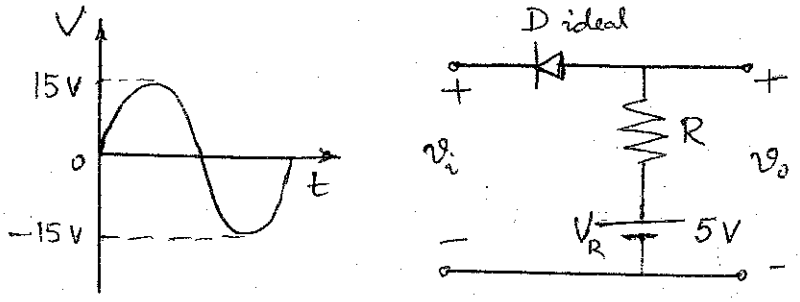

Fig 1(a).

b. Draw the circuit of a full wave bridge rectifier with capacitor filter and explain its operation. Derive an expression for its ripple factor. **(10 Marks)**

c. Explain the operation of a full wave voltage doubler circuit. **(05 Marks)**

2 a. Discuss the causes for bias instability in a transistor. **(05 Marks)**

b. Explain how a diode can be used in a transistor circuit to compensate for changes in V_{BE}. **(05 Marks)**

c. In the circuit of Fig 2(c) shown below, $V_{Cc} = 24V$, $R_c = 10K\Omega$, $R_e = 270\Omega$. If a silicon transistor is used with $\beta = 45$ and if under quiescent conditions $V_{CE} = 5V$, determine R and the stability factor S. **(10 Marks)**

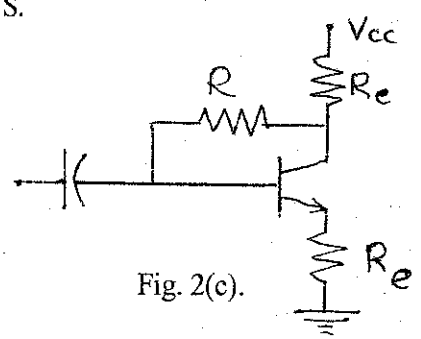

Fig. 2(c).

3 a. Draw the hybrid small signal model of a transistor and explain the significance of each component in the model. **(05 Marks)**

b. Using h-parameter model for a transistor in C.E configuration, Derive expressions for A_I, Z_i, A_V and Y_o of the amplifier. **(09 Marks)**

Contd....2

c. In the circuit of Fig 3(c) shown below, Calculate the input impedance R_i. The transistor parameters are hie = 1100Ω, hre = 2.5 x 10^{-4}, hoe = 25μ A/V. **(06 Marks)**

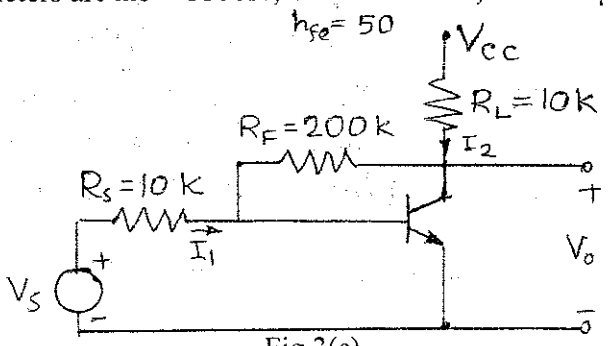

Fig 3(c)

4 a. State and prove Miller's theorem. **(05 Marks)**

b. Derive expressions for transistor input conductance $g_b{}'_e$ and output conductance g_{ce}. **(10 Marks)**

c. Discuss different types of distortions in amplifiers. **(05 Marks)**

5 a. Draw a feedback amplifier in block diagram form. Identify each block and explain their function. **(07 Marks)**

b. Derive expressions for input and output resistances of a current shunt feedback amplifier. **(08 Marks)**

c. An amplifier with an open loop voltage gain Av = 1000 ± 100 is available. It is necessary to have an amplifier whose voltage gain varies by no more than ± 0.1 percent. Find:
i) The reverse transmission factor β of the F.B network and
ii) The gain with F.B. **(05 Marks)**

6 a. Discuss different types of power amplifiers in terms of their efficiency and applications. **(05 Marks)**

b. Draw the circuit diagram of a class B push pull amplifier and explain the operation with relevant wave forms. Also derive the maximum conversion efficiency of this amplifier. **(10 Marks)**

c. Calculate the peak power dissipation in each transistor and the maximum power output in a class B push pull amplifier it V_{Cc} = 10V and $R_L^1 = 4\ \Omega$. **(05 Marks)**

7 a. Draw the circuit and explain how to measure the differential input resistance of an op. Amp. **(06 Marks)**

b. Design an op. Amp Schmitt trigger circuit to meet the following specifications. $V_{UTP} = 4V$, $V_{LTP} = -2V$, $V_O = \pm 12V$.

c. Explain the working of a D/A converter with R and 2R resistors. Derive the expression for the ouput voltage. **(08 Marks)**

8 a. Explain the working of an op. Amp positive clipper. **(06 Marks)**

b. Draw and explain the working of a Sample and Hold circuit. **(06 Marks)**

c. List the important features of 555 timer. Explain how an astable multivibrator using.555 timer can be used as a free- running ramp generator. **(08 Marks)**

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