NEW SCHEME

EE663

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Sixth Semester B.E. Degree Examination, July/August 2005

Electrical & Electronics Engineering

Digital System design Using VHDL

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer any FIVE full questions.*
2. Assume missing details if any.

1. (a) Describe the following with a suitable example

i) Symbol V_s Entity

ii) Configuration

iii) Event scheduling & Guarded block statement **(12 Marks)**

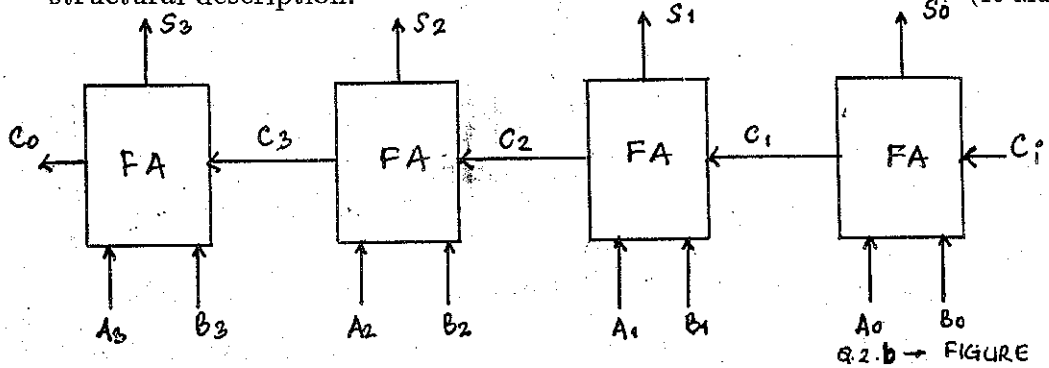
(b) Explain DATAFLOW style & BEHAVIORAL style of modeling in VHDL with an example of

$$Z = \overline{A}.B + A.C$$

Develop suitable VHDL code. **(8 Marks)**

2. (a) Explain TRANSPORT & INERTIAL DELAY MODEL in VHDL using an INVERTER with a delay of 20 nsecs. Develop VHDL code for above two models. Assume delay of wire = 10 nsecs. **(10 Marks)**

(b) For the 4 bit ADDER shown in the figure, write the VHDL code using structural description. **(10 Marks)**



Q.2.b → FIGURE

3. (a) Explain the following constructs with BNF, giving a suitable example

i) CASE statement ii) IF statement
iii) LOOP statement iv) WAIT statement

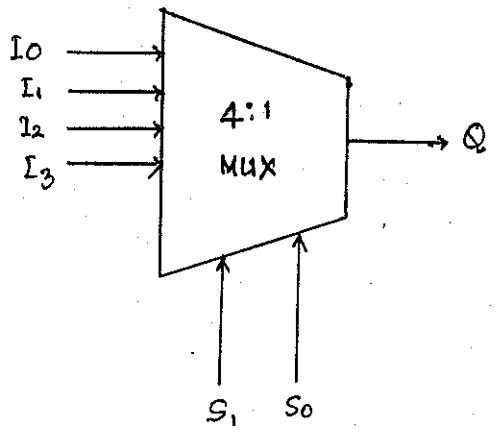
(12 Marks)

(b) Explain GENERICS in VHDL. Model an OR gate, using GENERICS by defining a delay of OR gate as parameter to the VHDL model. **(8 Marks)**

4. (a) Give the classification of DATA TYPEs in VHDL. Explain i) Scaler type of data with an example. **(12 Marks)**

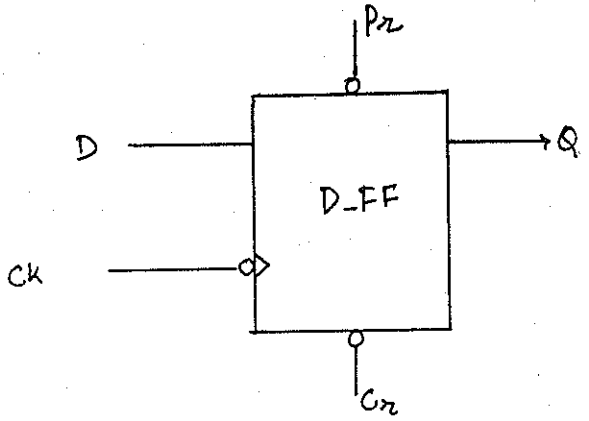
Contd.... 2

(b) Develop a VHDL code for the 4:1 MULTIPLEXER shown, using three - state logic **(8 Marks)**



5. (a) With BNF, clearly distinguish between FUNCTiONS & PROCEDURES in VHDL. Give a suitable example. **(10 Marks)**

(b) For the D-FLIP FLOP shown, write a VHDL code using a PROCESS statement having sensitivity list. **(10 Marks)**



6. (a) Explain package declaration & package body in VHDL with an example. **(10 Marks)**

(b) Write a BEHAVIORAL CODE for a 4 BIT-SHIFT-REGISTER using D-FLIP-FLOPS. **(10 Marks)**

7. (a) Explain register transfer level description with an example. **(10 Marks)**

(b) Develop a VHDL code to model an n bit synchronous binary counter using D FLIP FLOPS. Use generic to define n bit as a parameter having a value of 4, to the VHDL model. **(10 Marks)**

8. Write short notes on

a) File types b) Drivers
c) Statement concurrency d) Attributes

(4×5=20 Marks)

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EE663

Reg. No. | | | | | | | | | | |

Sixth Semester B.E. Degree Examination, January/February 2006

Electrical & Electronics Engineering

Digital System Design using VHDL

Time: 3 hrs.) (Max.Marks : 100

Note: ***Answer any FIVE full questions.***

1. **(a)** Explain the following with respect to VHDL with an example each.

i) Entity ii) Concurrent statement iii) Function iv) Array attribute **(8 Marks)**

(b) Bring out the differences clearly between the following VHDL statements :

i) $CLK <= not\ CLK\ after\ 20ns;$

ii) $CLK <= not\ CLK;$ **(6 Marks)**

(c) Narrate the following VHDL operators with examples

i) Binary logic operators

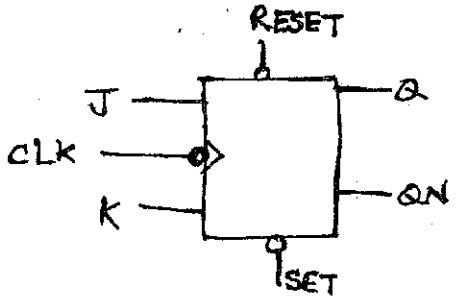
ii) Shift operators. **(6 Marks)**

2. **(a)** Summarise the sequence of events, when the following VHDL program is executed.

```
Process        (B, C, D)
begin
                A <= B; -- statement 1
                B <= C; -- statement 2
                C <= D; -- statement 3
end process ;
```

A, B, C and D are signals of type integer and are initialised to $A = 2$, $B = 4$, $C = 5$ and $D = 0$. D changes to 6 at time = 10 ns. **(6 Marks)**

(b) Model the J-K flip-flop shown in Fig 2.b using VHDL process.



(8 Marks)

(c) Distinguish between single dimensional array and multidimensional array with examples. **(6 Marks)**

3. **(a)** What are procedures ? How are they used in VHDL ? Explain. **(6 Marks)**

(b) Write a VHDL code for a 4 bit adder and briefly explain it. Use component declaration for the program. **(8 Marks)**

Contd.... 2

(c) Model the 4 : 1 MUX shown in Fig 3.(c) using 'case' statement.

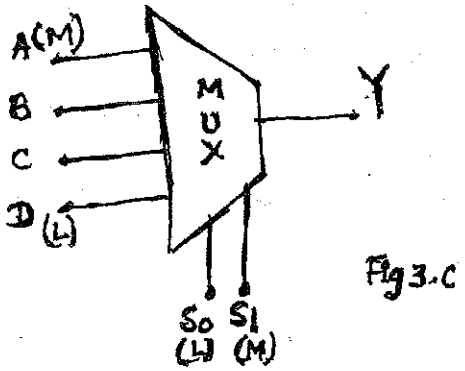


Fig 3.c

(6 Marks)

4. **(a)** Model an 8:3 encoder using VHDL and explain the same briefly. **(8 Marks)**

(b) Write a VHDL program to model a 4-bit comparator. **(8 Marks)**

(c) Write a note on packages. **(4 Marks)**

5. **(a)** For the flow chart shown in fig 5.a, use nested ifs and elsifs statements. Bring out the differences. S_1 to S_6 are sequential statements C_1, C_2 & C_3 are inputs to be tested. **(8 Marks)**

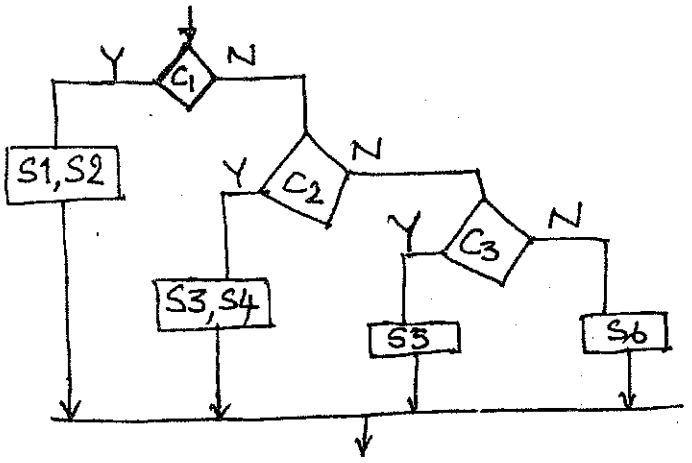


Fig 5.a

(b) Write a VHDL code for a 4 bit shift register with the following operations.

i) SISO

ii) PIPO

iii) PISO

iv) SIPO **(12 Marks)**

Contd.... 3

6. **(a)** Write a VHDL code for a 4 bit ripple counter, built using D flip-flops. **(8 Marks)**

(b) Write a state diagram for 011 sequence detector and explain. Write the VHDL code for the same. **(12 Marks)**

7. **(a)** What are FPGAs ? List the merits and demerits. **(6 Marks)**

(b) What are the different programming technologies with which a FPGA is fabricated? Explain. **(8 Marks)**

(c) Give the various steps involved in designing a digital system using FPGA. **(6 Marks)**

8. Write short notes on :

i) Test bench

ii) CPLD

iii) Synthesis of VHDL code

iv) CAD tools for digital system design **(4×5=20 Marks)**

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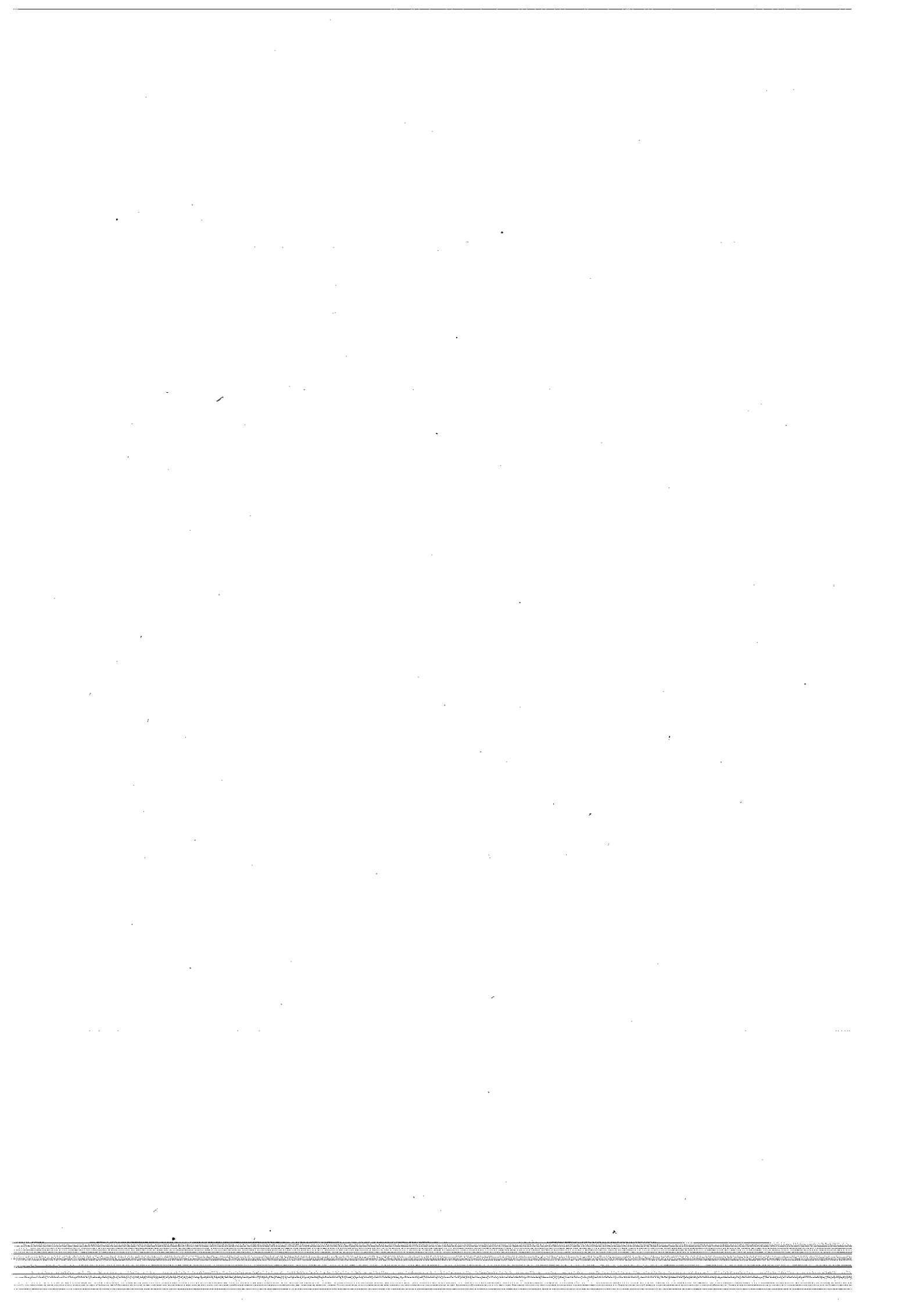

EE663

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NEW SCHEME

Sixth Semester B.E. Degree Examination, July 2007
Electrical & Electronic Engineering
Digital System Design Using VHDL

Time: 3 hrs. [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. What is the need for CAD tools? With reference to CAD tools discuss,
i) Design entity. ii) Synthesis.
iii) Functional simulation. iv) Physical design. **(15 Marks)**

b. Give the significance and analogy of entity – architecture sections of a VHDL code. **(05 Marks)**

2 List the three styles of modeling a digital system in VHDL. Give the VHDL code for each of them, with reference to half adder. **(20 Marks)**

3 a. List the seven classes of VHDL operators according to their precedence and indicate the order of evaluation of the expression,
A & not B or C nor 2 and D **(08 Marks)**

b. Write a VHDL code to implement a 2 : 4 decoder with an active low enable line using,
i) Conditional signal assignment. ii) Selected signal assignment statement.
Use '&' operator as required. **(12 Marks)**

4 a. Develop a VHDL code with generic and generate statement to model a N-bit parallel binary adder. **(10 Marks)**

b. What are inertial and transport delay models. Give their syntax and illustrate the difference between the two models. **(10 Marks)**

5 a. What are VHDL functions? Where do they appear? Give the complete VHDL code to find two's complement of a N-bit number. **(10 Marks)**

b. Write a VHDL code to model the Boolean expression,
$F(A, B, C) = \sum m(0, 3, 5, 6, 7)$
Using process statement. **(10 Marks)**

6 a. Write a VHDL code to model D flip-flop, assuming D, clock, preset and clear as the inputs and Q, Qbar as the output. Use process statement and no sensitivity list. **(08 Marks)**

b. Develop a VHDL code to model N-bit register that performs
i) Left shift. ii) Right shift. **(12 Marks)**

7 a. Give the VHDL code that models 4-bit up-down synchronous counter. **(08 Marks)**
b. Give the VHDL code that models 4-bit ring counter. **(08 Marks)**
c. What are packages in VHDL? Give an example. **(04 Marks)**

8 Discuss
a. Programmable logic devices. **(06 Marks)**
b. Structure of a CPLD. **(04 Marks)**
c. A 3-input LUT of a FPGA. **(06 Marks)**
d. Inclusion of a flip-flop in a FPGA logic block. **(04 Marks)**

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EE663

Sixth Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Digital System Design Using VHDL

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Describe the following with examples :
i) Architecture ii) Attributes iii) Generate statements. **(12 Marks)**
b. What is the difference between inertial delay and transport delay? Explain with an example. **(08 Marks)**

2 Explain the different styles of modeling in VHDL. Discuss the salient features of them taking the example of a full adder. **(20 Marks)**

3 a. Explain with examples the following constructs with BNF.
i) Case Statement ii) Wait Statement iii) Loop Statement. **(12 Marks)**
b. Write a VHDL code for 8:3 encoder operation. **(08 Marks)**

4 a. Discuss the various data types in VHDL with examples. **(12 Marks)**
b. Model a 3-8 decoder with enable input using VHDL. **(08 Marks)**

5 a. Explain different types of procedures with examples. **(10 Marks)**
b. Write the behavioral description to simulate 8 byte RAM with Read/write line, address data lines, and active low chip select line. Implement the read and write operations in the architecture.

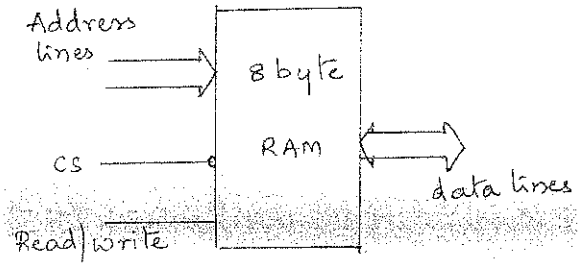

Fig.5(b) **(10 Marks)**

6 a. Explain package and package body. **(05 Marks)**
b. Write the behavioral code for a 4-bit universal register using D – FF and 4:1 multiplexer with control inputs S_0 and S_1 which specify the type of operation as shown in the table below. The block diagram representation of the universal shift register is shown in fig.6(b). **(15 Marks)**

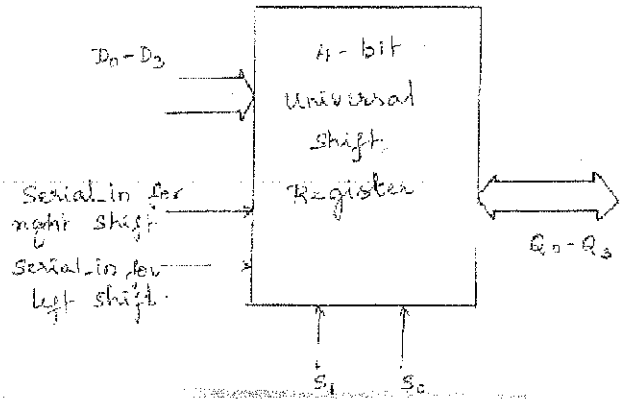

Fig.6(b)

S_1	S_0	Mode of operation
0	0	hold
0	1	shift right
1	0	shift left
1	1	Parallel load

Table 6(b)

7 a. Describe briefly the configuration statement with an example. **(08 Marks)**

b. Write the VHDL code to implement a synchronous counter having the counting sequence as 2, 0, 3, 1, 2, 0, 3, 1, ... using T - FF **(12 Marks)**

8 a. What are FPGAs? Discuss their features. **(08 Marks)**

b. Give the various steps involved in designing a digital system using FPGA with an example. **(12 Marks)**

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EE663

Sixth Semester B.E. Degree Examination, June/July 08
Digital System Design Using VHDL

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Explain in brief the evolution of VHDL and mention the capabilities of the language. **(08 Marks)**

b. Explain the following
   i) Entity
   ii) Architecture
   iii) Packages **(12 Marks)**

2 a. List the operators allowed in VHDL language. **(05 Marks)**

b. Explain the different styles of modeling using VHDL taking an example of half adder. **(15 Marks)**

3 a. Give the classification of data types and explain with examples
   i) Physical type
   ii) Enumerated type **(10 Marks)**

b. Write a VHDL code for 3-bit ripple up counter employing JK flip-flops using structural style of modeling. **(10 Marks)**

4 a. Explain the inertial and transport delays used in VHDL taking an example of buffer. **(10 Marks)**

b. Write a VHDL code for 4 to 1 MUX using selected and conditional signal assignment concurrent statements i.e WITH/SELECT/WHEN. **(10 Marks)**

5 a. Write the BNF for the following and explain with an example
   i) Loop
   ii) CASE
   iii) EXIT **(10 Marks)**

b. Write a VHDL code for positive edge triggered d-flip –flip with active high reset asynchronous input using guarded block statement. **(10 Marks)**

6 a. Explain the structure of process statement. **(08 Marks)**

b. Model JK flip flop that has active low direct inputs and responds to the falling edge of the clock using IF statement. **(12 Marks)**

7 a. Explain the FUNCTION and PROCEDURE with an example. **(10 Marks)**

b. What is FPGA? Explain the architecture of FPGA. **(10 Marks)**

8 a. Write a note on architecture of CPLD. **(10 Marks)**

b. Write a VHDL code for 8 – bit ripple adder using Loop statement. Use GENERICS. **(10 Marks)**

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