Sixth Semester B.E. Degree Examination, December 2010
Digital System Design using VHDL

Time: 3 hrs.   Max. Marks:100

Note: *Answer any FIVE full questions.*

1   a.   Distinguish between variables and signals. Give examples.   (04 Marks)
      b.   Write VHDL models for a 4-to-1 multiplexer.   (08 Marks)
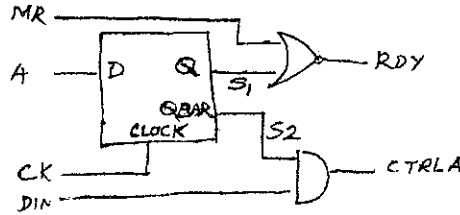   c.   Write VHDL structural model for the circuit shown in fig. Q1 (c).   (08 Marks)

Fig. Q1 (c)

2   a.   Discuss general model of mealy sequential machine. How do you realize mealy sequential network with a ROM?   (08 Marks)
      b.   What is programmable logic array? Give suitable example.   (08 Marks)
      c.   Explain assert statement and report statement. Give examples.   (04 Marks)

3   a.   Design a binary multiplier and hence write VHDL code (behavior model) for 4×4 binary multiplier.   (10 Marks)
      b.   Write a block diagram for signed divider with state graph for signed divider control network and write test bench for signed divider.   (10 Marks)

4   a.   With the help of case construct, write VHDL code for SM chart for binary multiplier.   (07 Marks)
      b.   Describe alternative realizations for SM charts using microprogramming.   (07 Marks)
      c.   Write a note on linked state machines.   (06 Marks)

5   a.   Mention the steps to be followed, when designing with FPGAS, a digital system.   (08 Marks)
      b.   Describe input output block-Xilinx 3000 series.   (04 Marks)
      c.   Discuss the features of Altera complex programmable logic devices (CPLDS).   (08 Marks)

6   a.   Explain multivalued logic and signal resolution with examples.   (08 Marks)
      b.   Distinguish between intertial delay and transport delay.   (04 Marks)
      c.   Describe synthesis of VHDL code with examples.   (08 Marks)

7   a.   Explain STATIC RAM memory. Write simple memory model in VHDL.   (10 Marks)
      b.   Explain how 486 bus interface is done to a memory system and hence draw SM chart for simplified 486 bus interface.   (10 Marks)

8   Write short notes on the following:
      a.   FPGA and CPLD.
      b.   Generics.
      c.   Operator overloading.
      d.   Package.   (20 Marks)

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