EC64

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Sixth Semester B.E. Degree Examination, July/August 2005

Electronics and Communication /Telecommunications Engineering

Digital System Design using VHDL

Time: 3 hrs.] [Max.Marks : 100

Note: *Answer any FIVE full questions.*
All questions carry equal marks.

1. (a) Write a behavioral description of JK flipflop with active low clock, set and reset using process statement. **(6 Marks)**

   (b) Write a data flow description for the given equation using process statement

   $(i/p : x,\ clk \qquad o/p : z) \qquad Z = X^1Q_3^1 + XQ_3$

   $Q_1^+ = Q_2^1\ ;\ Q_2^+ = Q_1\ ;\ Q_3^+ = Q_1Q_2Q_3 + X^1Q_1Q_3^1 + X\ Q_1^1\ Q_2^1$ **(8 Marks)**

   (c) Differentiate between signal assignment and variable assignment with a suitable example. **(6 Marks)**

2. (a) Evaluate the given expression. Is it true ?

   (A and not B or c ror 3 and D) = "1 0 0 0 1 1" where A="1 0 1" : B="0 1 1" ; c="1 0 0 0 1 0" ; D="1 1 0 0 1 0" **(6 Marks)**

   (b) Specify the declaration form for package and package body with an example. **(6 Marks)**

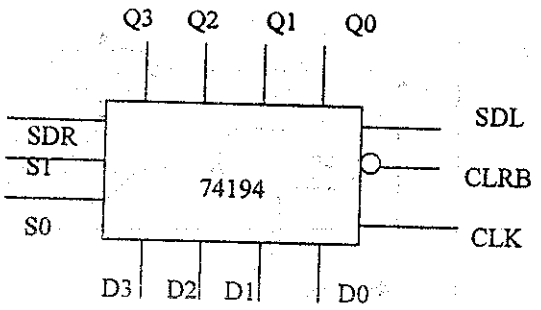
   (c) Write a VHDL description for a SR latch.

   i) use a conditional assignment statement

   ii) Use a characteristic equation

   iii) Use two logic gates **(8 Marks)**

3. (a) Write a VHDL description for a 74194 4-bit bi-directional shift register. **(8 Marks)**



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(b) Find the reduced PLA table to realize the following functions :

$f_1(a,b,c,d) = \sum m\ (4,5,10,11,12)$

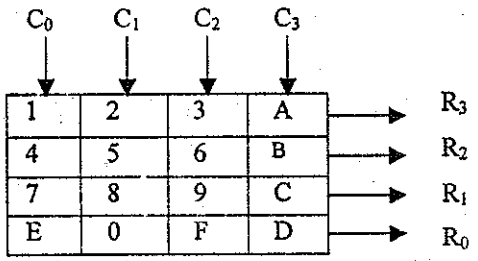
$f_2(a,b,c,d) = \sum m\ (0,1,3,4,8,11)$ and

$f_3(a,b,c,d) = \sum m\ (0,4,10,11,14)$ (6 Marks)

(c) Write a VHDL code for 4-bit adder with Rise/Fall time modeling using generic statement. (6 Marks)

4. (a) Implement the traffic-light controller using 74163 counter with added logic. Use a ROM to generate the o/ps. (6 Marks)

(b) Design a keypad scanner for the following keypad layout



(8 Marks)

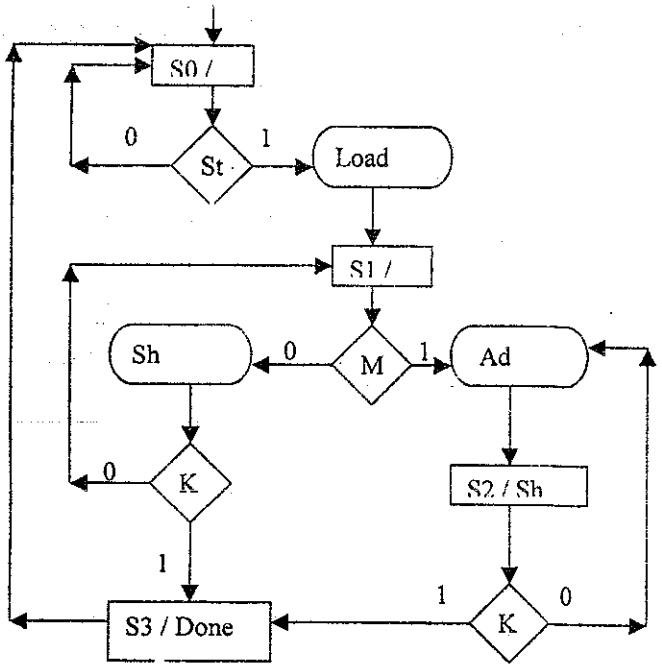
(c) Bring out the differences between transport delay and internal delay with suitable examples. (6 Marks)

5. (a) Design a 4-bit binary multiplier and generate the control state graph and table which defines the operation of a binary multiplier. (8 Marks)

(b) Realize the control circuit of 4-bit serial multiplier using a PLA and D flip flops. (8 Marks)

(c) Write a VHDL code for 2 input Nor gate with Rise/Fall time modeling using generic statement. (4 Marks)

6. (a) Write a VHDL description for 4-bit binary multiplier for the SM chart as shown below. (8 Marks)

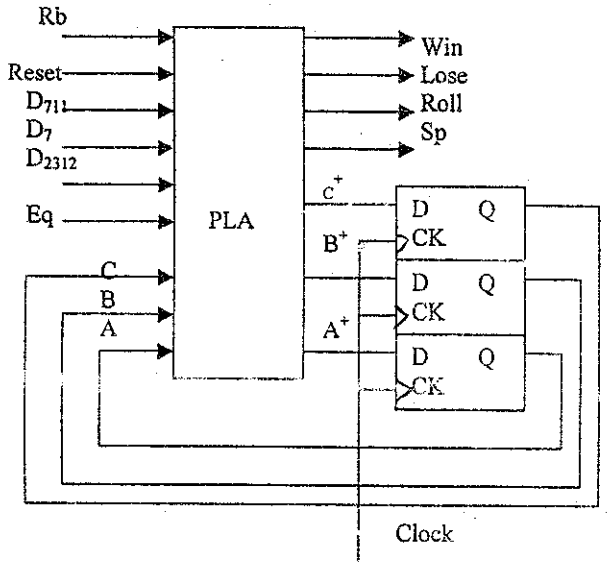


Contd.... 3

(b) Write a VHDL description for a divider that divides an 8-bit dividend by a 5-bit divisor to give a 3-bit quotient. The dividend register should be loaded when St=1. **(8 Marks)**

(c) Write a VHDL code for synthesis of a sequential IF statement. **(4 Marks)**

7. (a) The PLA realization of a Dice game is as shown in figure. Write a VHDL code for the same. **(8 Marks)**



(b) Implement a 4×4 array multiplier using Xilinx 4000 series. **(6 Marks)**

(c) Write a behavioral description of RAM 6116 using process statement. **(6 Marks)**

8. (a) Implement a 8-1 Mux using an Altera 7000 series device. Give the logic equations and determine the number of macro cells required if parallel expanders are used. **(6 Marks)**

(b) Write a VHDL code for the floating point subtracter. **(6 Marks)**

(c) Write a VHDL model for an N-bit bi-directional shift register using a generic statement. Define a component that represents one bit of the shift register. The component port should be port (L,R, CLR, CLK, Pin, Lin, Rin: in bit; Q : out bit) ; such that LR = 0 0 , do nothing ; LR = 01, shift right : LR=10, shift left and LR=11 parallel load. **(8 Marks)**

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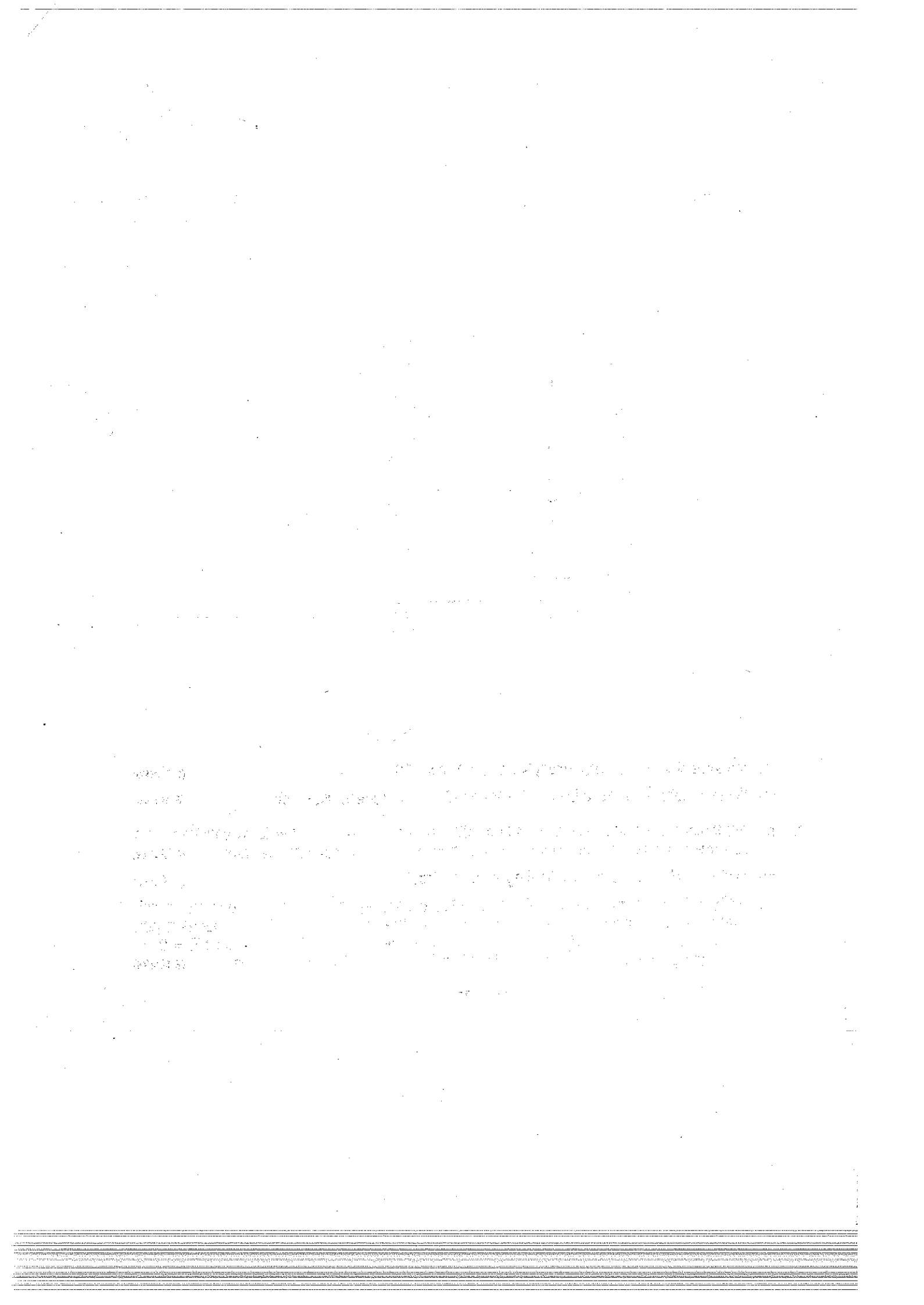


NEW SCHEME

EC64

Reg. No. | | | | | | | | | | |

Sixth Semester B.E. Degree Examination, January/February 2006

Electronics & Communication/Telecommunication Engineering

Digital System Design Using VHDL

Time: 3 hrs.) (Max.Marks : 100

Note: ***Answer any FIVE full questions.***

1. **(a)** Explain briefly :

i) Entity architecture pair

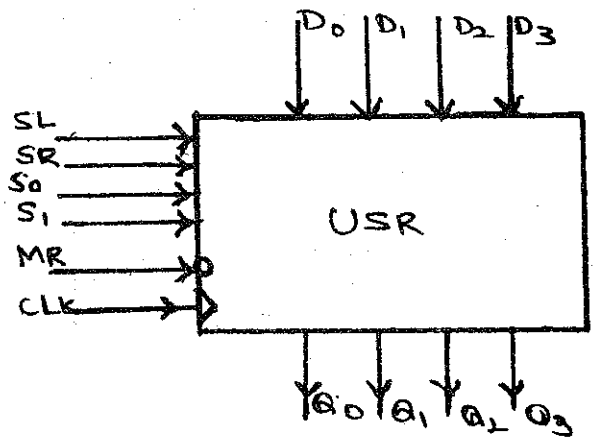
ii) Package in VHDL. **(5+5 Marks)**

(b) Write a VHDL code for a full subtracter using logic equation. **(6 Marks)**

(c) If A=1100, B=1110, C=1001, compute Y_1 = not A and B nor 2
Y_2 = B sla 2 and C sll 2. **(4 Marks)**

2. **(a)** What is meant by variables, signals and constants in VHDL? Compare signals with variables, give an example for each. **(10 Marks)**

(b) Write a VHDL module for a universal shift register with following functions. MR Active low, a synchronous reset I/P that resets all flipflops. Two control inputs (S_1S_0) when 00, no action, when 10, register is shifted right and serial data SR enters Q_0, when 01, 4 bit data shifted left and SL enters Q_3. If $S_1S_0 = 11$, 4 bit data is loaded parallely. **(8 Marks)**



(c) Specify the general form of case statement. **(2 Marks)**

3. **(a)** Realize the following functions using PLA.

$F_1 = \sum m(2,3,5,7,8,9,10,11,13,15)$

$F_2 = \sum m(2,3,5,6,7,10,11,14,15)$

$F_3 = \sum m(6,7,8,9,13,14,15)$

Write VHDL code for implementation of F_1, F_2 *and* F_3. **(6+6 Marks)**

Contd.... 2

(b) Write a VHDL code for D flipflop that reports error for setup and hold time violation. Assume set up time = hold time = 5ns and display text string as violation of setup Or hold time. **(8 Marks)**

4. (a) Write state diagram that generates control signals for 4x4 bit multiplier. Explain with block diagram. **(8 Marks)**

(b) Design signed multiplier and write a VHDL code to multiply two signed numbers. **(6+6 Marks)**

5. (a) Derive a SM chart to realize DICE game. **(10 Marks)**

(b) Using PLA and D flip flops realize the SM chart for the dice game. **(10 Marks)**

6. (a) Explain briefly with neat sketch Kilink 3000 series I/O block. **(8 Marks)**

(b) Write a function Fadd ion VHDL to realize full adder operation. Design 4 bit parallel adder using full adders and write behavioral model for 4 bit parallel adder that uses function Fadd. **(6+6 Marks)**

7. (a) What is meant by attributes. Explain signal attribution with an example for each. **(2+6 Marks)**

(b) Write a VHDL code for T flipflop. Using T flipflop as component write structural model for 8 bit up counter. Assume active low asynchronous clear input and falling edge triggered clock.
Use Generate statement **(2+4 Marks)**

(c) Write a VHDL module for memory model (RAM6116). Assume 8 bit address lines, 8 bit data lines, active low chip enable and active low write enable. **(6 Marks)**

8. Write short notes on any FOUR :

(a) Transport and inertial delay

(b) Generic

(c) Signal resolution

(d) Modeling mealy machine

(e) VHDL procedures. **(5×4=20 Marks)**

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NEW SCHEME

Sixth Semester B.E. Degree Examination, July 2006
E & C
Digital System Design using VHDL

Time: 3 hrs.] [Max. Marks:100

Note: Answer any FIVE full questions.

1 a. Explain structural and behavioral description with examples. **(08 Marks)**

b. Differentiate between : i) Signal and variable assignment
ii) Event and transactions. **(06 Marks)**

c. Write a VHDL program for detecting the number of 1's in an eight bit-vector. If even, it should output 'O'; if odd, output = '1'. **(06 Marks)**

2 a. If A = 110101 B = 110010 , compute (A S112) OR (B S1A3) **(04 Marks)**

b. A Moore sequential machine with two inputs x1 and x2 and output z has the following state table.

State	X1 X2				Z
	0 0	0 1	1 0	1 1	
1	1	1	2	2	0
2	1	2	2	1	1

Write the VHDL code at behavioral level. State changes occur after 5 ns and output changes occur 5 ns after state changes. **(08 Marks)**

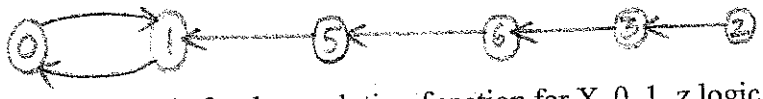
c. Realize using ROM and DFF and write the VHDL code using ROM table for

PS	NS		
	W = 0	W = 1	Z
0 0	0 0	0 1	0
0 1	0 0	1 0	0
1 0	1 0	0 1	0
1 1	1 0	0 1	1

(08 Marks)

3 a. Find a minimum row PLA table to implement the following sets of functions
f_1 (A,B,C,D) = $\sum$m (3,4,6,9,11)
f_2 (A,B,C,D) = $\sum$m (2,4,8,10,11,12)
f_3 (A,B,C,D) = $\sum$m (3,6,7,10,11)
and realize these functions using a PLA. **(06 Marks)**

b. A counter has the count sequence as shown. Realise the counter using 16 R4 PAL. Draw the section of the PAL where this function is implemented.



(10 Marks)

c. Write a VHDL code for the resolution function for X, 0, 1, z logic. **(04 Marks)**

Contd...2

4 a. Draw and explain the block diagram of a 3 digit BCD to binary converter and draw the state graph for the same. **(08 Marks)**

b. Draw the block diagram, state graph and VHDL program for the behavioral model of a 4 x 4 multiplier. **(12 Marks)**

5 a. Design and explain an 8 bit divider wherein dividend is 8 bit and divisor is 4 bit. The shift and subtract action should take place in the same cycle. Draw the block diagram and state diagram. **(10 Marks)**

b. Give the contents of the dividend register with respect to clock cycle for the given dividend and divisor. Shift and subtract in separate clock cycles.
Dividend – 0 1 1 1 0 0 0 0 1 0 divisor 1 0 0 0 1 **(10 Marks)**

6 a. For the following Sm chart give the timing diagram showing the clock, states , input and output. Give the PLA table.

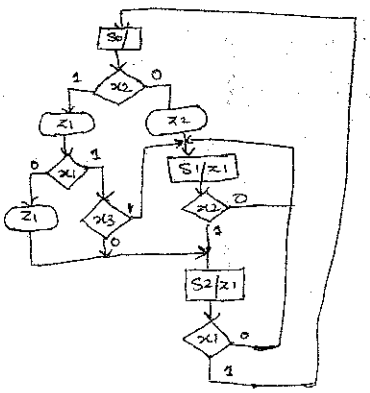


Fig. 6 (a) **(10 Marks)**

b. Implement a bit binary counter using one Xilinx 3000 series logic cell. Qx is the LSB bit and Qy is the MSB of the counter. The counter has an asynchronous reset and a synchronous load. The counter operates as follows :

En = 0 no change
En = 1 . Ld = 1 load Qx and Qy with inputs u and v
En = 1 Ld = 0 2 increment count

i) Give the next state equations for Qx and Qy
ii) Label the inputs on the FG mode diagram and show the connection paths.
(10 Marks)

7 a. Write a VHDL code for a static Ram with truth table **(08 Marks)**

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	mode	I/o pins
H	X	X	not selected	high z
L	H	H	output disabled	high z
L	L	H	read	data out
L	X	L	write	Data in

b. Write a VHDL function that will find the dot product $\sum ai * bi$ of two integer vectors a and b. **(06 Marks)**

c. Explain signal attributes with examples. **(06 Marks)**

8 a. Explain the Xilinx 3000 series logic cell **(07 Marks)**

b. Explain transport and inertial delays with examples. **(06 Marks)**

c. Write a VHDL code and synthesized circuit for case statement. **(07 Marks)**

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EC64

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NEW SCHEME

Sixth Semester B.E. Degree Examination, Dec. 06 / Jan. 07
EC / TE
Digital System Design Using VHDL

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Using a single bit subtractor, write a VHDL code for 4-bit subtractor. **(08 Marks)**

b. Differenciate between the conditional assignment statement and single assignment statement with respect to 4 : 1 Mux. **(06 Marks)**

c. What are the predefined unconstrained arrays? Explain each with an example. **(06 Marks)**

2 a. Bring out the differences between VHDL function and VHDL procedure with an example. **(06 Marks)**

b. Draw the structure of a 8-bit counter using 74163. Write a VHDL description for a 8-bit counter using 74163 model. **(08 Marks)**

c. Write a VHDL code for synthesis of a sequential CASE statement. **(06 Marks)**

3 a. Write a VHDL description that converts a 5-bit bit_vector to an integer. **(08 Marks)**

b. Realize the following functions using PLA : **(06 Marks)**

$f_1(a,b,c,d) = \sum m(2,3,5,7,8,9,10,11,13,15)$,

$f_2(a,b,c,d) = \sum m(2,3,5,6,7,10,11,14,15)$ and $f_3(a,b,c,d) = \sum m(6,7,8,9,13,14,15)$

c. Model the tristate buffers with active – high output enable. **(06 Marks)**

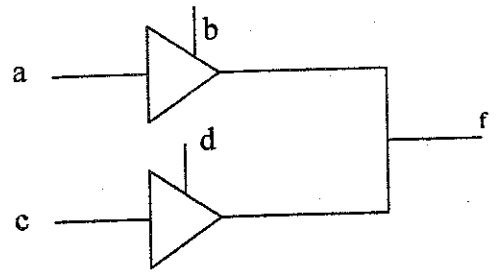
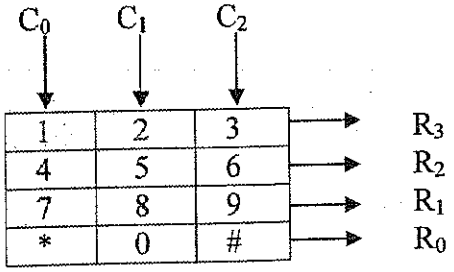


Fig.3(c)

4 a. Design a 6-bit binary up-down counter using a 22V10 and a minimum number of external gates. Write the VHDL code for the counter using PLA. **(10 Marks)**

b. Design a keypad scanner for the following keypad layout. **(10 Marks)**



Contd...2

5 a. Design a 4-bit serial adder with accumulator and generate the control state graph and table which defines the operation of a serial adder. **(08 Marks)**

b. Write a VHDL module that describes one bit of a full adder with accumulator . The control i/p Ad = 1 add operation and Load = 1 load the i/p to the accumulator. **(06 Marks)**

c. Write a VHDL code for 2 input Nor gate with Rise / Fall time modeling using generic statement. **(06 Marks)**

6 a. Write a test-bench for the Dice game problem to test the game components. **(10 Marks)**

b. The functional equivalent of a static RAM cell is as shown in figure. Write a VHDL code to realize the functionality **(10 Marks)**

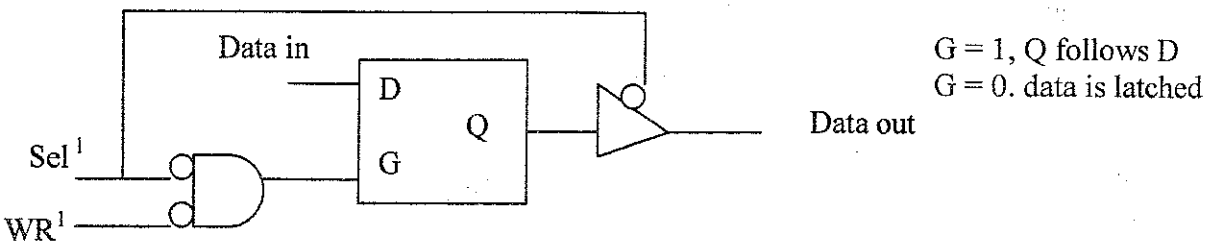


Fig. 6(b)

7 a. Give sequence of simulator commands that would test the divider for the case 93 divided by 17. **(06 Marks)**

b. Write a VHDKL code for the resolution function for X 0 1 Z logic. **(06 Marks)**

c. Realize the SM chart given using a PLA, counter and 4-1 Mux. **(08 Marks)**

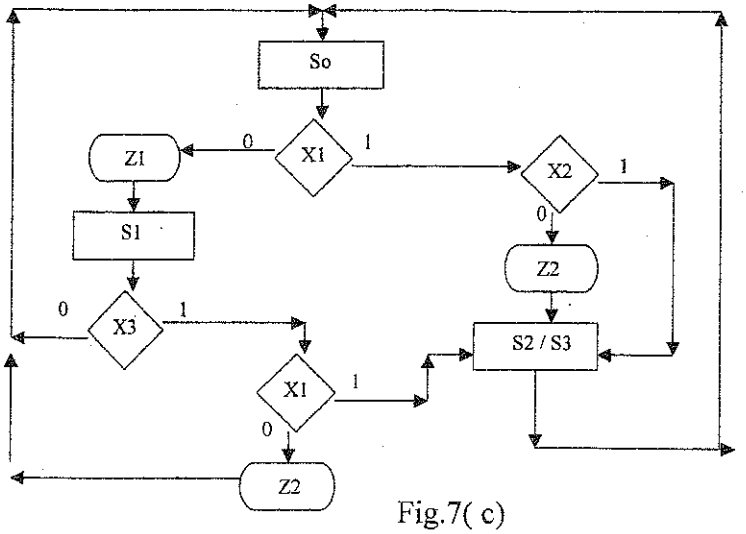


Fig.7(c)

8 a. Show how to realize the following combinational function using two 3000 series logic cells. **(10 Marks)**

$F = X_1^1 X_2 X_3^1 X_6 + X_2^1 X_3^1 X_4 X_6^1 + X_2 X_3^1 X_4^1 + X_2 X_6 X_4^1 X_6 + X_3^1 X_6 X_4 X_5 X_6^1 + X_7$

b. Write a VHDL code using One-hot assignment for the following specifications

To : Q0 Q1 Q2 Q3 = 1000 ; T1 = 0100 ; T2 = 0010 ; T4 = 0001

$Q3^+ = X1\ Q0 + X2\ Q1 + X3\ Q2 + X4\ Q3$; $Z1 = X1\ Q0 + X3\ Q2$;

$Z2 = X2\ Q1 + X4\ Q3$; **(10 Marks)**

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NEW SCHEME

Sixth Semester B.E. Degree Examination, Dec. 06 / Jan. 07
EC / TE
Digital System Design Using VHDL

Time: 3 hrs.] [Max. Marks:100

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2 a. Bring out the differences between VHDL function and VHDL procedure with an example. **(06 Marks)**

b. Draw the structure of a 8-bit counter using 74163. Write a VHDL description for a 8-bit counter using 74163 model. **(08 Marks)**

c. Write a VHDL code for synthesis of a sequential CASE statement. **(06 Marks)**

3 a. Write a VHDL description that converts a 5-bit bit_vector to an integer. **(08 Marks)**

b. Realize the following functions using PLA : **(06 Marks)**

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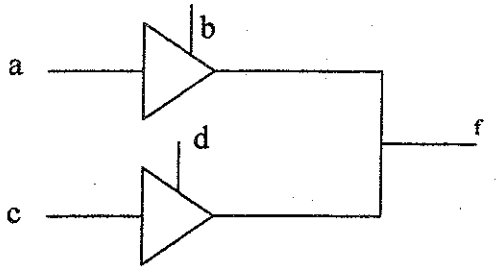

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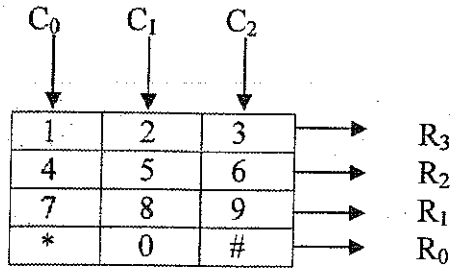

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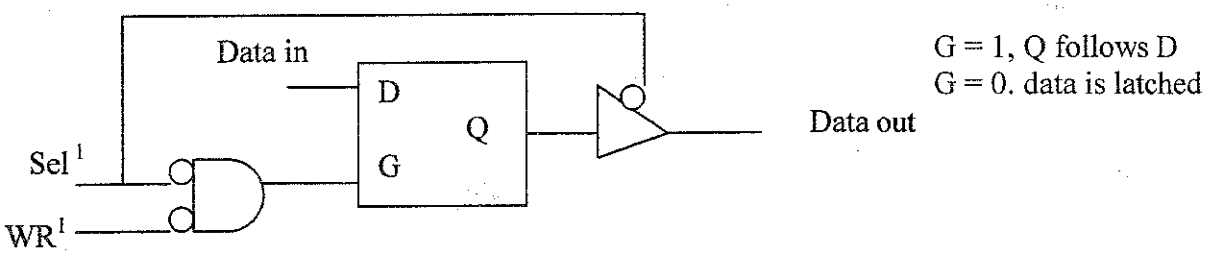

Fig. 6(b)

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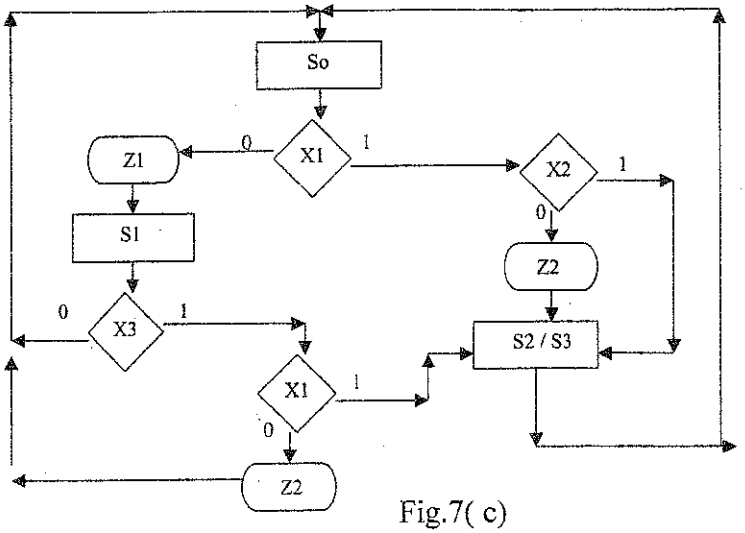

Fig.7(c)

8 a. Show how to realize the following combinational function using two 3000 series logic cells. **(10 Marks)**

$F = X_1^{\,1} X_2 X_3^{\,1} X_6 + X_2^{\,1} X_3^{\,1} X_4 X_6^{\,1} + X_2 X_3^{\,1} X_4^{\,1} + X_2 X_6 X_4^{\,1} X_6 + X_3^{\,1} X_6 X_4 X_5 X_6^{\,1} + X_7$

b. Write a VHDL code using One-hot assignment for the following specifications

To : Q0 Q1 Q2 Q3 = 1000 ; T1 = 0100 ; T2 = 0010 ; T4 = 0001

$Q3^{+} = X1\ Q0 + X2\ Q1 + X3\ Q2 + X4\ Q3$; $Z1 = X1\ Q0 + X3\ Q2$;

$Z2 = X2\ Q1 + X4\ Q3$; **(10 Marks)**

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EC64

USN | | | | | | | | | | |

NEW SCHEME

Sixth Semester B.E. Degree Examination, July 2007
EC / TE
Digital System Design Using VHDL

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Write down the VHDL-code to model the following :
   i) D-flip flop
   ii) J-K flip flop
   iii) 4 : 1 multiplexer **(09 Marks)**

b. Starting from a single bit full adder as a component, write down the structural VHDL description for a 4 bit adder. **(06 Marks)**

c. With the help of a block diagram, explain the stages of compilation, elaboration and simulation. **(05 Marks)**

2 a. Develop the VHDL code for 8 bit counting using IC 74163 binary synchronous counters. Show the hardware diagram. **(06 Marks)**

b. Explain with a set of statements, the sequential execution using process and if else statements. Assume suitable delays wherever necessary. **(06 Marks)**

c. Implement a Mealy sequential network with ROM and D-flip flops for BCD to excess 3 code convertor. Draw the ROM truth table and ROM realization code. **(08 Marks)**

3 a. Using CMOS-PLD 22CE V10, design a VHDL code for a sequential traffic light controller. Supply the necessary state graph and state table. **(10 Marks)**

b. For a keypad scanner (4 rows × 3 columns), develop a VHDL code incorporating key bouncing. Supply the stategraph for scanner and truth table for decoder. **(10 Marks)**

4 a. Draw the state graph for binary multiplier control and hence develop a behavioral VHDL model for binary multiplier. **(10 Marks)**

b. Draw the block diagram for a signed divider (32 bits by 16 bits) with the associated control circuits. Supply the steps of procedure to carry out the division. Draw the state graph for control circuit. **(10 Marks)**

5 a. Describe the design of a serial adder with accumulator supplying the block diagram control state graph and state table. **(10 Marks)**

b. Derive an SM chart for the control of unsigned binary multiplier (4 bits × 4 bits). Convert this SM chart into VHDL code. **(10 Marks)**

Contd.... 2

6 a. For the dice game based on the following rules, draw the SM chart and develop the behavioral VHDL code.

i) After the first roll of the dice the player wins if the sum is 7 or 11. The player loses if the sum is 2, 3 or 12. Otherwise, the sum the player obtained on the first roll is referred to as a point and he or she must roll the dice again.

ii) On the second or subsequent roll of the dice, the player wins if the sum equals the point, and he or she loses if the sum is 7. Otherwise, the player must roll again until he or she finally wins or loses. **(10 Marks)**

b. With Xilinx XC 3020, implement a parallel adder-subtractor with an accumulator. Show a typical logic design cell with inputs and outputs, and signal paths shown after programming. **(10 Marks)**

7 a. Assuming that configuration data is available in EPROM, outline the steps of procedure to design any digital system using FPGA. Give one example of design. **(10 Marks)**

b. Explain IEEE-1164 standard logic system for use with VHDL taking one VHDL code example. **(10 Marks)**

8 a. Develop a VHDL code for a RAM system with data register, memory control and MAR, giving block diagram and the corresponding SM chart. **(10 Marks)**

b. Write the separate SM charts for simplified 486 bus interface with CPU and for UART receiver. **(10 Marks)**

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EC64

Sixth Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Digital System Design Using VHDL

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Explain the following with declaration format and an example each:
i) Variable ii) Signal iii) Constant **(06 Marks)**

b. Using a process statement write a VHDL source code for 4 to 1 multiplexer. **(06 Marks)**

c. Bring out differences between a VHDL function and a VHDL procedure with a suitable example. **(08 Marks)**

2 a. The data stored in the ROM location are (9, A, 0, 0, 1, 0, 0, 1, F, C, C, D, 7, 4, 6, 7). Write a VHDL code for the ROM realization by using the binary values of the numbers given above. **(06 Marks)**

b. Find a minimum row PLA table to implement the following set of functions.

$f_1(A,B,C,D) = \sum m(3,4,6,9,11)$

$f_2(A,B,C,D) = \sum m(2,4,8,10,11,12)$

$f_3(A,B,C,D) = \sum m(3,6,7,10,11)$ **(09 Marks)**

c. A keypad has 4 rows and 3 columns as shown in figure Q2 (c)

1	2	3
4	5	6
7	8	9
*	0	#

Fig. Q2 (c)

Assume no more than two keys will be pressed at a time. Write the block diagram of keypad scanner and first 10 rows of the truth table for a keypad decoder. If 2 keys are pressed in the same column, the N output should indicate the key in the first of the 2 rows. **(05 Marks)**

3 a. With a neat block diagram and the function tables, explain the operation of a serial adder with accumulator. **(06 Marks)**

b. The state graph for faster multiplex (4 × 4) is as shown in figure Q3 (b). Write a behavioral model (VHDL source code) for 2's complement 4 × 4 binary multiplier. **(07 Marks)**

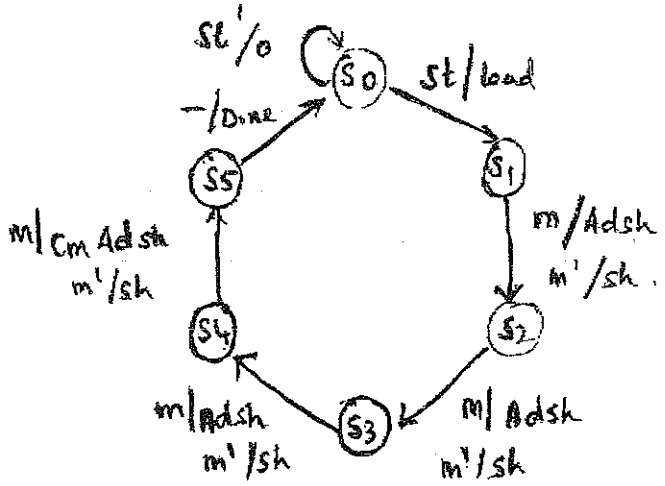

Fig. Q3 (b)

3 c. Design a binary divider and draw the block diagram of the same. Show the procedure t divide 135 by 13 [convert it into binary and perform the operations]. **(07 Marks**

4 a. Derive the state machine (SM) chart for dice game and obtain the state graph for dice gam controller. **(10 Marks**

b. Write a VHDL description of the state machine band on SM chart. **(10 Marks**

Present state	Next state				Output z_1 z_2			
	x_1 x_2 =00	01	10	11	x_1 x_2 =00	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

5 a. Explain in brief with necessary SM charts, the linked state machines. **(06 Marks**

b. Discuss the programmable interconnects between the CLB (Configurable Logic Blocks and I/O blocks with respect to

i) General purpose interconnects.

ii) Direct interconnects. **(08 Marks**

c. With a neat diagram explain the CLB as a Read / Write memory cell of Xilinx 4000 serie FPGA. **(06 Marks**

6 a. Design a floating point multiplier, explicitly showing the exponent adder, fractio multiplier and control network. **(10 Marks**

b. Explain operator over loading and write a source code for VHDL package with overloade operation for bit-vectors. **(06 Marks**

c. Write a VHDL code for the following tristate buffers with active – high output enabl (figure Q6 (c)). **(04 Marks**

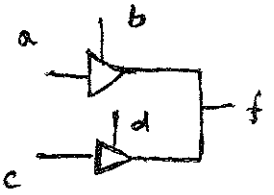

Fig. Q6 (c)

7 a. Write a VHDL source code to 4 bit adder using generate statement. **(04 Marks)**

b. With a neat block diagram and truth table explain the 6116 static RAM. **(07 Marks)**

c. Explain the simplified 486 bus model with a microprocessor bus interface and timing diagram of intel 486 basic 2 – 2 bus cycle. **(09 Marks)**

8 Write short notes on:

a. Compilation / Simulation.

b. VHDL operators.

c. Synthesis.

d. Programmable Array Logic (PALs). **(20 Marks)**

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EC64

Sixth Semester B.E. Degree Examination, June/July 08
Digital System Design Using VHDL

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Declaring all the inputs of a 4 × 1 MUX as vectors write VHDL codes with same entity but different architecture using the following constructs of the language :
i) with – select ii) if – then – else iii) when – else iv) case – clause **(10 Marks)**

b. Model a priority encoder with inputs W_3, W_2, W_1 and W_0. Input W_3 has the highest priority while W_0 has the lowest priority. Encoder output is a two-bit code (Y_1 Y_0). There is an extra output Z, which is set to zero when all inputs are equal to zero. Use standard logic type of VHDL objects in your code. **(06 Marks)**

c. Bring out the differences between VHDL functions and procedures. **(04 Marks)**

2 a. Write a VHDL procedure Addrec, which will add two N-bit vectors and a carry and returns an N-bit sum and a carry. The procedure call is of the form
Addrec (A, B, Cin, Sum, Cout, N); **(06 Marks)**

b. Write a VHDL program to detect the number of ones in an 8-bit vector. The output of the detector must be '0' for even number of ones, while '1' for odd number of ones. **(06 Marks)**

c. Model behaviourally the following 2-digit BCD counter :

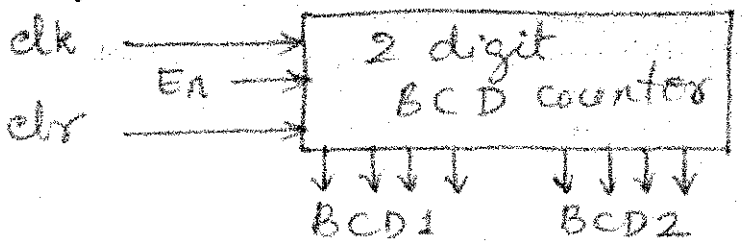

Fig.2(c) **(08 Marks)**

3 a. An N-bit bi-directional shift register has N parallel data inputs, N outputs, a Left Serial Input (LSI), a Right Serial Input (RSI), a clock input and the following control signals :
Load : load the parallel data into the register (load overrides shift)
Rsh : Shift the register right (LSI goes into the left end)
Lsh : Shift the register left (RSI goes into the right end)
If the register is implemented using PAL 22V10, what is the maximum value of N? **(10 Marks)**

b. A mealy sequential network with four output variables is realized using a 22V10. What is the maximum number of input variables it can have? The maximum number of states? Can any mealy network with these number of inputs and outputs be realized with a 22V10? Explain. **(10 Marks)**

4 a. With the state graph of binary multiplier control, write the behavioral model for 4 × 4 binary multiplier. **(10 Marks)**

b. Write a VHDL module that describes one bit of a full adder with accumulator. The module should have two control inputs, A_d and L. If $A_d = 1$, the Y input (and carry input) are added to the accumulator. If L = 1, the Y input is loaded into the accumulator. Using this module write a VHDL description of a 4-bit subtractor with accumulator. Assume negative numbers are represented in 1's complement. The subtractor should have control signal inputs S_u (subtract) and L_d (load). **(10 Marks)**

5 a. Construct an SM chart equivalent to following state table. Test only one variable in each decision box. Try to minimize the number of decision boxes.

Present state	Next state				Outputs Z_1Z_2				
	$X_1X_2 = 00$	01	10	11	$X_1X_2 =$	00	01	10	11
S_0	S_3	S_2	S_1	S_0		00	10	11	01
S_1	S_0	S_1	S_2	S_3		10	10	11	11
S_2	S_3	S_0	S_1	S_1		00	10	11	01
S_3	S_2	S_2	S_1	S_0		00	00	01	01

(10 Marks)

b. Write a VHDL description of the state machine based on the SM chart of Q.No.5(a). **(10 Marks)**

6 a. With the block diagram, explain the Configurable Logic Block (CLB) of Xilinx 3000 series logic cell in FPGA. **(10 Marks)**

b. Explain the architecture of Altera 7000 series CPLD. **(10 Marks)**

7 a. With sample waveforms explain transport and inertial delays in VHDL. **(08 Marks)**

b. Explain the use of generics in VHDL. **(06 Marks)**

c. Write the VHDL code for the synthesis of a case statement. **(06 Marks)**

8 a. Write a simple VHDL model for the memory that does not take timing considerations into account. **(10 Marks)**

b. Write an SM chart for simplified 486 bus interface. **(10 Marks)**

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2002 SCHEME

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EC64

Sixth Semester B.E. Degree Examination, Dec.09-Jan.10
Digital Systems Design using VHDL

Time: 3 hrs. Max. Marks:100

Note: 1. ***Answer any FIVE full questions.***
2. ***Standard notations are used.***

1 a. Write VHDL code for a full subtracter using logic equations and using this module as a component, develop VHDL code for a 4-bit subtracter. **(10 Marks)**

b. Develop a VHDL model for a simple heater thermostat using PROCESS. The model has two integer inputs, one that specifies the desired temperature and another that is connected to a thermometer, and one boolean output that turns a heater ON and OFF. The thermostat turns the heater ON if the measured temperature falls below two degrees less than the desired temperature, and turns the heater OFF if the measured temperature rises above two degrees greater than the desired temperature. **(05 Marks)**

c. With suitable examples, compare variables and signals in VHDL. **(05 Marks)**

2 a. A Moore sequential machine with two inputs (x_1 and x_2) and one output (z) has the following state table :

PS	NS				Z
	x_1 x_2 = 0 0	x_1 x_2 = 0 1	x_1 x_2 = 1 0	x_1 x_2 = 1 1	
1	1	2	2	1	0
2	2	1	2	1	1

Write VHDL code that describes the machine at the behavioral level. Assume that the state changes occur 10 ns after the rising edge of the clock and output changes occur 10 ns after the state changes. **(08 Marks)**

b. Write a procedure for adding two N-bit vectors and a carry, and returns N-bit sum and carry. The procedure call should be of the form addvec(A,B,C in, Sum, Cont, N) **(05 Marks)**

c. Write a behavioral level VHDL model for the 4-bit bidirectional shift register 74194. The description of 74194 is as follows :
The CLRb input is asynchronous and active low and overrides all the other control inputs. All other state changes occur following the rising edge of the clock. If the control inputs S_1=S_0=1, the register is loaded in parallel. If S_1=1 and S_0=0, the register is shifted right and SDR (serial data right) is shifted into Q_3. If S_1=0 and S_0=1, the register is shifted left and SDL (serial data right) is shifted into Q_0. If S_1=S_0=0, no action occurs. **(07 Marks)**

3 a. The following state table is implemented using a ROM and two D flip flops (falling edge):

Q_1	Q_2	Q_1^+ x = 0	Q_2^+ x = 1	Z x = 0	Z x = 1
0	0	0 1	1 0	0	1
0	1	1 0	0 0	1	1
1	0	0 0	0 1	1	0

Draw the block diagram. Write VHDL code that describes the system. Assume that the ROM has a delay of 10 ns, and each flip flop has a propogation delay of 15 ns. **(08 Marks)**

b. Find a minimum row PLA table to implement the following set of functions :
$f_1(A,B,C,D) = \sum m(4,5,10,11,12)$; $f_2(A,B,C,D) = \sum m(0,1,3,4,8,11)$
$f_3(A,B,C,D) = \sum m(0,4,10,12,14)$
And draw the figure showing the PLA realization of equations f_1, f_2 and f_3. **(07 Marks)**

c. With a neat block diagram, describe the operation of a parallel adder with accumulator. Discuss with related equations, how many bits of the parallel adder and accumulator can be fit into a PAL 22v10? **(05 Marks)**

4 a. Draw the block diagram, state graph and write VHDL behavioral model for 4 x 4 binary multiplier. **(08 Marks)**

b. Draw the block diagram and state graph for signed divider. Write VHDL model of signed divider for 32-bit divider and 16-bit divider. **(12 Marks)**

5 a. The block diagram for multiplier control and state graph for add-shift control are shown in Fig.Q5(a1) and Fig.Q5(a2) respectively. The counter counts the number of shifts and outputs K=1 just before the last shift occurs. The add-shift control generates the required sequence of add and shift signals. Derive the state machine chart and write VHDL code for control of the binary multiplier.

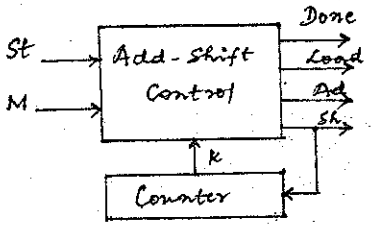

Fig.Q5(a1)

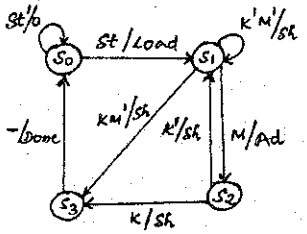

Fig.Q5(a2) **(10 Marks)**

b. Derive the SM chart for the dice game and write VHDL behavioral model for the dice game using its SM chart. **(10 Marks)**

6 a. Implement a 2-bit binary counter using one Xilinx series logic cell. Q_x is the least significant bit, and Q_y is the most significant bit of the counter. The counter has an a synchronous reset (AR) and a synchronous load (Ld). The counter operates as follows :

En = 0	No change
En = 1, Ld = 1	Load Q_x and Q_y with external inputs u and v on rising edge of clock.
En = 1, Ld = 0	Increment counter on rising edge of clock.

i) Give the next state equations for Q_x and Q_y.

ii) Label the inputs on the FG mode diagram and show the connection path. **(08 Marks)**

b. With a simplified block diagram, describe the Xilinx 4000 series CLB. Also, draw the diagram to show how a CLB can be configured as a 16 x 2-bit RAM. **(12 Marks)**

7 a. With a neat block diagram, explain the operation of floating point multiplier which consists of an exponent adder and a fraction multiplier. **(08 Marks)**

b. Differentiate inertial delay and transport delay, with an example. **(04 Marks)**

c. Using GENERIC statement write VHDL code for a three input nandgate. Consider T_{rise}, T_{fall} and load in your model. Also, write a VHDL structural model that contains two instances of your nandgate, where in the first instance works with T_{rise} = 2 ns, T_{fall} = 1 ns and load = 2, second instance uses default values specified. **(08 Marks)**

8 a. Draw the block diagram and write VHDL code for static RAM model with truth table Q8(a).

$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Mode	I/O pins
H	X	X	Not selected	high-Z
L	H	H	Output disabled	high-Z
L	L	H	Read	data out
L	X	L	Write	data in

Table Q8(a) **(10 Marks)**

b. What is operator overloading? Write VHDL package with overloaded operators for bit-vectors. **(10 Marks)**