2002 SCHEME

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CS82

Eighth Semester B.E. Degree Examination, December 2010
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions.***

1 a. Discuss the evolution of computer architecture, with a suitable diagram. **(10 Marks)**

b. Explain the vector super computer, with a neat diagram. **(10 Marks)**

2 a. Briefly explain the different types of data dependencies. For the following code segment, draw the dependency graph:

S_1 : Load R_1, A ; $R_1 \leftarrow$ Mem(A)
S_2 : Add R_2, R_1 ; $R_2 \leftarrow [R_1] + [R_2]$
S_3 : Mov R_1, R_3 ; $R_1 \leftarrow [R_3]$
S_4 : Store B, R_1 ; Mem(B) $\leftarrow [R_1]$ **(08 Marks)**

b. Compare control flow architecture and data flow architecture. **(06 Marks)**

c. List the node degree, number of links and network diameter for the following:
i) Completely connected
ii) Binary tree
iii) 2D Mesh
iv) 2D Torus **(06 Marks)**

3 a. Compare the superscalar processor and VLIW processor. **(08 Marks)**

b. Consider the following interleaved memory design for a main memory system with 16 memory modules. Each module is assumed to have a capacity of 1 Mbyte. The machine is byte addressable.

Design 1 : 8-way interleaving with 2 memory banks.
Design 2 : 4-way interleaving with 4 memory banks.

i) Specify the address format for each of the above memory organizations.
ii) Determine the maximum memory bandwidth obtained, if only one memory module fails, in each of the above organizations. **(06 Marks)**

c. Explain the overlapping register window mechanism of SPARC architecture. **(06 Marks)**

4 a. With a neat diagram, explain the back plain bus. **(10 Marks)**

b. Design a binary integer multiply pipeline with 5 stages. The first stage is for partial product generation. The last stage is a 36b carry-lookahead adder. The middle 3 stages are made of 16 carry-save adder of appropriate lengths.

i) Prepare a schematic design of 5-stage multiply pipeline. All line widths and inter-stage connection must be shown.
ii) Determine the maximal clock rate of the pipeline of the stage delays are $t_1 = t_2 = t_3 = t_4 = 90$ ns and $t_5 = 45$ ns. The latch delay is 20 ns.
iii) What is the maximal throughput of this pipeline in terms of the number of 36b results generated per second? **(10 Marks)**

5 a. Indicate the factors that could cause delays in the instruction pipeline. For one of the listed factors, explain how the pipeline delay can be reduced. **(10 Marks)**

b. Consider the following pipeline reservation table:

	1	2	3	4
S_1	X			X
S_2		X		
S_3			X	

i) What are the forbidden latencies?
ii) Draw the state transition diagram.
iii) List all simple cycles and greedy cycle.
iv) Determine minimum average latency.
v) Find the optimal constant latency cycle.
vi) Determine the throughput of this pipeline, with clock period being 20 ns.
(10 Marks)

6 a. What is the cache-coherence problem? Explain Goodman's write-once cache coherence protocol. **(10 Marks)**

b. What is a barrier? Explain the hardware method of implementing the barrier. **(10 Marks)**

7 a. In a supermarket, vendors would be interested in extracting the information on the item sets, the customers frequently purchase, using the large database, indicating set of items purchased in each transaction. Show how this information of frequently purchased item sets could be obtained. Explore the parallelism that exists in the process. **(10 Marks)**

b. Write the parallel code for the simple equation solver, using the message-passing model. **(10 Marks)**

8 a. With the necessary diagrams, explain the following types of message passing protocols:
i) Asynchronous
ii) Synchronous **(12 Marks)**

b. What is meant by a scalable system? Explain any two types of scaling. **(08 Marks)**

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