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06CS81

Eighth Semester B.E. Degree Examination, May/June 2010
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define computer architecture. Illustrate the seven dimensions of an ISA. **(08 Marks)**

b. What is dependability? Explain two main measures of dependability. **(06 Marks)**

c. Given the following measurements:

Frequency of FP operations = 25% Average CPI of FP operations = 4.0

Average CPI of other instructions = 1.33 Frequency of FPSQR = 2%

CPI of FPSQR = 20

Assume that the two design alternatives are to decrease the CPI of FPSQR to 2 or to decrease the average CPI of all FP operations to 2.5. Compare the two design alternatives using the processor performance equations. **(06 Marks)**

2 a. With a neat diagram, explain the classic five-stage pipeline for a RISC processor. **(10 Marks)**

b. What are the major hurdles of pipelining? Illustrate the branch hazards in detail. **(10 Marks)**

3 a. What are the techniques used to reduce branch costs? Explain both static and dynamic branch prediction used for same. **(10 Marks)**

b. With a neat diagram, give the basic structure of Tomasulo based MIPS FP unit and explain the various fields of reservation stations. **(10 Marks)**

4 a. Explain the basic VLIW approach for exploiting ILP, using multiple issues. **(10 Marks)**

b. What are the key issues in implementing advanced speculation techniques? Explain them in detail. **(10 Marks)**

PART – B

5 a. Explain the basic schemes for enforcing coherence in a shared memory multiprocessor system. **(10 Marks)**

b. Explain the directory based coherence for a distributed memory multiprocessor system. **(10 Marks)**

6 a. Assume we have a computer where the clocks per instruction (CPI) is 1.0 when all memory accesses hit in the cache. The only data accesses are loads and stores and these total 50% of the instructions. If the mass penalty is 25 clock cycles and the mass rate is 2%, how much faster would the computer be if all instructions were cache hits? **(10 Marks)**

b. Explain in brief, the types of basic cache optimization. **(10 Marks)**

7 a. Which are the major categories of advanced optimizations of cache performance? Explain any one in detail. **(10 Marks)**

b. Explain in detail, the architecture support for protecting processes from each other via virtual memory. **(10 Marks)**

8 a. Explain in detail, the hardware support for preserving exception behaviour during speculation. **(10 Marks)**

b. Explain the prediction and speculation support provided in IA64. **(10 Marks)**

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