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06CS81

Eighth Semester B.E. Degree Examination, December 2012
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer FIVE full questions atleast TWO questions from each part.***

PART – A

1 a. List and explain four important technologies which have led to the improvements in computer system. **(10 Marks)**

b. Give a brief explanation about trends in power in integrated circuits and cost. **(10 Marks)**

2 a. Explain the pipeline hazards, in detail. **(10 Marks)**

b. Show java loop is unrolled so that there are four copies of the loop body, assuming $R_1 - R_2$ (that is, the size of the array) is initially a multiple of 32, which means that the number of loop iterations is a multiple of 4. Eliminate any obviously redundant computations and do not reuse any of the registers. **(10 Marks)**

3 a. What is dynamic prediction? Draw the state transition diagram for 2 bit prediction scheme? **(04 Marks)**

b. What is the basic complier technique for exposing ILP? **(06 Marks)**

c. How to overcome the data hazards with dynamic scheduling? **(10 Marks)**

4 a. How do exploit ILP, using multiple issues and dynamic scheduling? **(10 Marks)**

b. What is the basic concept of VLIW approach? **(10 Marks)**

PART – B

5 a. Explain the symmetric shared memory architecture, in detail. **(10 Marks)**

b. Explain in detail, the distributed shared memory and directory based coherence. **(10 Marks)**

6 a. How to protect virtual memory and virtual machines? **(10 Marks)**

b. Assume that the hit time of a two –way set-associative first –level data cache is 1.1 times faster than a four-way set-associative cache of the same size. The miss rate falls from 0.049 to 0.044 for an 8 KB data cache. Assume a hit is 1 clock cycle and that the cache is the critical path for the clock. Assume the miss penalty is 10 clock cycles to the L2 cache for the two-way set-associative cache, and that the L2 cache does not miss. Which has the faster average memory assess time? **(05 Marks)**

c. Suppose you measures a new DDR3 DIMM to transfer at 16000 MB/sec. what do you think its name will be? What is the clock rate of that DIMM? What is your guess of the name of DRAMS used in that DIMM? **(05 Marks)**

7 a. Describe eleven advanced optimizations for cache performance. **(12 Marks)**

b. What is memory technology and optimization? **(08 Marks)**

8 a. How to enhance the loop level parallelism? **(10 Marks)**

b. What all are the hardware support for exposing parallelism? **(10 Marks)**

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