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06CS81

Eighth Semester B.E. Degree Examination, December 2011
Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Define the computer architecture. Explain the response time, throughput, elapsed time and processor clock. **(06 Marks)**

b. Briefly explain the Amdahl's law. **(07 Marks)**

c. Two code sequences for a particular machine are considered by a compiler designer.

Instruction class	CPI for this instruction class
A	1
B	2
C	3

The compiler designer considers 2 code sequences that require the following instruction counts for a particular high – level language statement.

Code sequence	Instruction counts for instruction class		
	A	B	C
1	20	10	20
2	40	10	10

i) Which code sequence executes most of the instructions?
ii) What is the CPI for each sequence?
iii) Which will be faster? **(07 Marks)**

2 a. What are the major hurdles of pipelining? Illustrate the data hazard, briefly. **(10 Marks)**

b. With a neat block diagram, explain how an instruction can be executed in 4 or 5 clock cycles in MIPS data path, without the pipeline register. **(10 Marks)**

3 a. List the steps to unroll the code and schedule. **(05 Marks)**

b. Explain how Tomasulo's algorithm can be extended to support speculation. **(10 Marks)**

c. Explain the dynamic branch prediction state diagram. **(05 Marks)**

4 a. Explain the basic VLIW approach. List its drawbacks. **(08 Marks)**

b. With a neat diagram, explain the steps involved in handling an instruction, with a branch target buffer. Also evaluate how well it works. **(12 Marks)**

PART – B

5 a. Explain the different taxonomy of parallel architecture. **(08 Marks)**

b. With a neat diagram, explain the basic structure of a centralized shared – memory and distributed – memory multiprocessor. **(06 Marks)**

c. Explain the snooping, with a respect to cache – coherence protocols. **(06 Marks)**

6 a. Explain the six basic optimizations. **(12 Marks)**

b. With a neat diagram, explain the hypothetical memory hierarchy. **(08 Marks)**

7 a. Explain the DRAM technology. How do you improve memory performance inside a DRAM chip? **(10 Marks)**

b. Explain the compiler optimizations to reduce miss rate. **(10 Marks)**

8 a. Find all the true dependences, output dependences and antidependences and eliminate the output and antidependences by renaming, in the code given below:

```
for (i = 1;   i <= 100;  i = i + 1) {
    y[i] = x[i] /c ;      /* s1 */
    x[i] = x[i]+c ;       /* s2 */
    z[i] = y[i]+c ;       /* s3 */
    y[i] = c – y[i] ;     /* s4 */
    }
```

(10 Marks)

b. Write short notes on:

i) The Itanium 2 processor

ii) IA – 64 register model. **(10 Marks)**

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