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CS82

Eighth Semester B.E. Degree Examination, Dec. 07 / Jan. 08

Advanced Computer Architecture

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Mention the two categories of parallel computers and explain them with their architecture. **(10 Marks)**

b. Explain the different types of data dependence with an example for each. **(10 Marks)**

2 a. Trace out the following program to detect parallelism using Bernstein's conditions.

P_1 : $C = D \times E$
P_2 : $M = G + C$
P_3 : $A = B + C$
P_4 : $C = L + M$
P_5 : $F = G \div E$

Assume that each step requires 1 step to execute and 2 adders are available. Compare between sequential and parallel execution of the above program. **(07 Marks)**

b. Define the following terms :
i) Grain packing ii) Coarse grain and iii) Fine grain. **(06 Marks)**

c. Explain how grain packing can be done to compute the sum of the 4 elements in the resulting product matrix $C = A \times B$ where matrices A and B are of order 2×2. **(07 Marks)**

3 a. Discuss and compare the characteristics of CISC and RISC architectures. **(10 Marks)**

b. Discuss and compare the following : **(10 Marks)**
i) Base scalar processing. ii) Super scalar processing and iii) Pipelining technique.

4 a. With respect to shared memory organization, explain the memory interleaving technique. **(10 Marks)**

b. Explain set – associative cache organization and discuss on its design trade offs. **(10 Marks)**

5 a. For the non-linear pipeline having the reservation table shown below, find the following :
i) Greedy cycle ii) Latency cycle iii) Minimum average latency cycle.
iv) State – Transition Diagram. **(10 Marks)**

	1	2	3	4	5	6	7	8
S_1	X					X		X
S_2		X		X				
S_3			X		X		X	

b. With respect to mechanisms for instruction pipelining, explain internal data forwarding and possible hazard between read and write operations. **(10 Marks)**

6 a. Draw an 8×8 Omega network using 2×2 switches. From your network show the followin simultaneous connections between input and output. **(10 Marks**

I/P :	0	4	3	6	7	5	2	1
O/P :	6	7	0	4	3	1	2	5

Is the network blocked or not? If it is blocked, how can you resolve the conflicts?

b. What do you mean by cache coherence problem? Explain the role of snoopy bus protocol related to this problem. **(10 Marks**

7 a. With respect to parallel programs, explain parallelization process and parallelizatio computation versus data. **(08 Marks**

b. Explain various parameters used under scalable multiprocessors for scalability. **(08 Marks**

c. Discuss any one case study for parallel application. **(04 Marks**

8 Write short notes on :

a. VLIW architecture. **(07 Marks**

b. Arithmetic pipeline design. **(07 Marks**

c. Control flow versus data flow. **(06 Marks**

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