CS46

NEW SCHEME

USN

Fourth Semester B.E. Degree Examination, July/August 2004

BM/EC/IT/TE/ML/EE/CS/IS

Computer Organisation

Time: 3 hrs.] [Max.Marks : 100

Note: *1. Answer FIVE Questions.*
2. All questions carry equal marks.

1. (a) Consider the memory system of a computer storing the following data :

Address in Hex	Data stored (binary)
2000	00111000
2001	00110100
2002	00110010
2003	00111001

Interpret the storage as numbers in the manner indicated below and find their decimal values in each case.

i) Big-endian storage of 2 hex words of 4 - digits each

ii) Big-endian storage of 2 BCD words of 4 - digits each.

iii) Little - endian storage, in ASCII, of a 4 - digit signed hex word.

iv) Little endian storage, in ASCII, of a 4 - digit BCD word. **(2 $\frac{1}{2}$×4=10 Marks)**

(b) Give reasons to justify using, generally,

i) Single address instructions in 8 - bit CPU's

ii) Double address instruction in 16-bit CPU's

iii) Three address instructions in RISC systems

In each of these systems give assembly language programs for performing the operation :

data at mem A + data at meb B → memC. **(10 Marks)**

2. (a) What do you understand by stack frames ? Discuss their use in sub-routines. **(10 Marks)**

(b) Write an assembly program to multiply 2 memory arrays and store their result in a third memory array :

$a(i) * b(i) = c(i)$ for $i = 0$ to $n - 1$.
Consider load/store and 3-address system. **(10 Marks)**

3. (a) Explain how interrupt request from several I/O devices can be communicated to a processor through a single INTR line.

(b) Which type of I/o devices are interfaced through DMA ?
Explain the bus-arbitration process used for DMA. **(10 Marks)**

Contd.... 2

4. (a) Explain the general features of interfacing a parallel I/o port to a processor. **(10 Marks)**

(b)

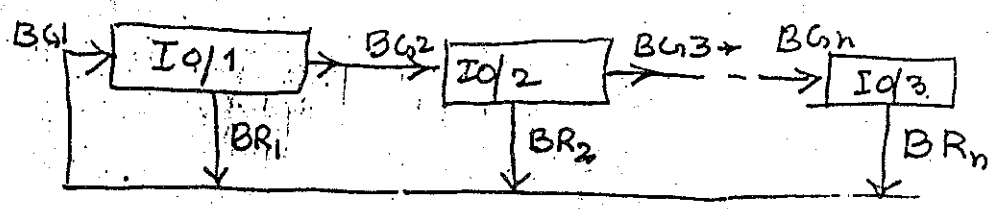

Fig Q 4b)

Consider the daisy chain arranement shown in fig Q.4b in which the bus request signal from the I/O is directly fed back as bus grant signal. Assume device IO/3 requests the bus and begins using it. When the device is finished, it deactivates BR3. Assume the delay from BG_i to BG_{i+1} in any device is d. Show that a spurious bus-grant pulse will travel down stream from device 3. Estimate the width of this pulse. **(10 Marks)**

5. (a) Describe SDRAM and DDR SD RAM operations for data transfer between main memory and cache memory systems. **(10 Marks)**

(b) Consider a processor running a program 30% of the instructions of which require a memory read or write operation if the cache bit ratio is 0.95 for instructions and 0.9 for data. When a cache bit occurs for instruction or for data, only one clock is needed while the cache miss penalty is 17 clocks to read/write on the main memory. Work out the time saved by using the cache, given the total number of instructions executed is 1 million. **(10 Marks)**

6. (a) Work out the multi level look - ahead carry scheme for doing a 32 bit number addition How many gate delays are required to do the complete addition in this method ? **(10 Marks)**

(b) The hexa decimal value of π is 3.243F6A8885A308D3... Work out the IEEE standard representation (IEEE standard 754-1985) of π in single and double precision formats. **(5+5 Marks)**

7. (a) Show the basic organisation of a CPU in terms of registers and other units for a single bus data path CPU. In such a CPU, show the complete action of the CPU in fetching and executing the instruction.

Load R_1 from memory data at A, where A is a memory address. Assume the instruction is in one process or word. Indicate the control signals to be used at each stage of execution. **(10 Marks)**

(b) Explain the basic concept of micro programmed control. **(10 Marks)**

8. (a) With a block diagram explain the general requirements of a microwave oven **OR** a digital camera. **(10 Marks)**

(b) Write short notes on any TWO.

i) A good method of hardware multiplication

ii) SCSI bus

iii) Virtual memory **(5+5 Marks)**

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CS46

NEW SCHEME

USN

Fourth Semester B.E. Degree Examination, January/February 2005
Common to BM/EC/EE/TE/ML/IT/CS/IS
Computer Organisation

Time: 3 hrs.] [Max.Marks : 100

Note: ***Answer any FIVE full questions.***

1. (a) Explain different functional units of a digital computer. **(6 Marks)**

(b) List and explain the developments made during different generations of computer. **(8 Marks)**

(c) What is a bus? Explain single bus structure in an architecture. **(6 Marks)**

2. (a) Explain the following :

i) Byte addressability

ii) Big-endian assignment **(6 Marks)**

iii) Little-endian assignment.

(b) What is an addressing mode? Explain different addressing modes. **(8 Marks)**

(c) What are assembler directives? Explain any two directives. **(6 Marks)**

3. (a) Explain i) Logical ii) Shift iii) Rotate instructions with examples. **(6 Marks)**

(b) Explain with an example, usage of stacks in a nested subroutine calls. **(8 Marks)**

(c) Write an assembly language program to solve an expression $ax^2 + bx + c = 0$ using two addressing modes. **(6 Marks)**

4. (a) Explain any two methods of handling multiple I/O devices. **(6 Marks)**

(b) Why bus arbitration is required? Explain with block diagram bus arbitration using daisy chain. **(8 Marks)**

(c) With a block diagram, explain, how a keyboard is connected to a processor. **(6 Marks)**

5. (a) How read and write operation takes place in $1K \times 1$ memory chip? Explain. **(6 Marks)**

(b) Explain any two cache mapping functions. **(8 Marks)**

(c) What are the keyfactors that affect the performance and cost of a computer with respect to memory? Explain briefly. **(6 Marks)**

6. (a) Explain the working principles of magnetic disk. **(8 Marks)**

(b) Give Booth's algorithm to multiply two binary numbers. Explain the working of algorithm taking an example. **(12 Marks)**

Contd.... 2

7. (a) Show the control sequences for execution of Add (R3), R1 and explain. **(6 Marks)**

(b) Explain the IEEE standards for floating point number. **(8 Marks)**

(c) With block diagram, explain the working of microwave oven in an embedded system. **(6 Marks)**

8. Write short notes on : **(5×4=20 Marks)**

i) Microprogrammed V/s hardwired control

ii) Virtual memory

iii) SCSI bus

iv) Multiprocessors and multi computers.

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NEW SCHEME

CS46

USN | | | | | | | | | | |

Fourth Semester B.E. Degree Examination, July/August 2005

Common to BM/EC/EE/TE/ML/IT/CS/IS

Computer Organisation

Time: 3 hrs.] [Max.Marks : 100

Note: ***Answer any FIVE full questions.***
All questions carry equal marks.

1. (a) Discuss the various generations through which the computers have evolved to the present stage. Indiate the important technological features and devices that characterised each generation. **(10 Marks)**

(b) Distinguish between unsigned and signed integers. With examples, indicate when each type of integers will be useful. **(4 Marks)**

(c) An integer of 32 bit size is stored in memory location in the little endian fashion. Indicate using a pseudo program, how a big endian 16-bit processor could rearrange the number and store it property for its use, back in the same location. **(6 Marks)**

2. (a) Using register transfer notation, and concept of indirect addressing of memory, show how you can rearrange an ascending sorted data array to a descending sorted array in the same memory locations. Assume the array elements are of 16-bit size, and the processor system is also 16 bit size. **(10 Marks)**

(b) Consider the following :

i) A subroutine may required the parameters passed to it (from the main program), in a random order and more than once.

ii) A stack is a data structure in memory, from which the data can be accessed in a lIFO order and obviously ten stack is not a suitable data structure for handling subroutine parameters.

iii) Yet, passing subroutine parameters through stack is perhaps the commonest way of handling subroutine parameters.

What mechanism is employed so that the parameters are made randomly accessible to the subroutine from the stack? Explain with an example. **(10 Marks)**

3. (a) Show a circuit arrangement, whereby several devices may interrupt a processor on a single interrupt request line.

If it is required to handle the device interrupts on a fixed priority basis, indicate in detail

i) A hardware based method

ii) A software based method for addressing this requirement. **(10 Marks)**

(b) Explain the hardware registers that are required in a DMA controller chip. Why is it necessary for a DMA controller to be able to interrupt the processor? Explain. **(10 Marks)**

Contd.... 2

4. (a) Explain the significant features of any ONE of the following bases :

i) PCI ii) SCSI iii) USB. **(10 Marks)**

(b) Discuss the different types of RAM's bringing out their salient features. Give some idea of their speeds and relative costs. **(10 Marks)**

5. (a) Consider a processor system with 32 bit address capability, using 64 KB of cache, arranged to operate as a 4 way set associative cache. Work out the logic which determines cache hit or miss for this system. Assume you have 20-bit comparators available for the purpose. **(10 Marks)**

(b) Describe the circuit and operation of a 4 bit carry look ahead adder. Compare the computational time, in terms of gate propagation times for a 32 bit adder using

i) 8 numbers of 4-bit carry look-ahead adders.

ii) 4 numbers of 8-bit carry look-ahead adders.

Assume no second level of look-ahead-carry generation. **(10 Marks)**

6. (a) Indicate the computational details of multiplying two 4-bit numbers 1011 and 0101 using Booth's algorithm. Verify the result obtained. **(10 Marks)**

(b) Give the basic features of the IEEE floating point number standard. **(10 Marks)**

7. (a) Give the details of the system and the control signals for executing the following functions in a processor

i) $MOV\ R_1\ to\ R_2$

ii) $LD\ M_1\ to\ R_2\ \ or\ \ ADD\ R_1\ to\ R_2.$ **(10 Marks)**

(b) Give a brief out line of the sequence of actions produced by a processor to fetch and execute an unconditional branch instruction in terms of the specific control signals produced at each clock during the whole process . **(10 Marks)**

8. (a) Indicate the various steps in designing either the hardwired control for a microprocessor or microprogrammed control for a microprocessor. **(10 Marks)**

(b) Describe the salient features of a simple microcontroller that can be embedded in systems like microwave ovens. **(10 Marks)**

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NEW SCHEME

CS46

Reg. No.

Fourth Semester B.E. Degree Examination, January/February 2006

Common to BM/EC/EE/TE/ML/IT/CS/IS

Computer Organisation

Time: 3 hrs.) (Max.Marks : 100

Note: *1. Answer any FIVE full questions.*

2. All questions carry equal marks.

1. (a) Explain in brief the evolution of computer system. **(6 Marks)**

   (b) What is pipelining? How does it improve the performance? **(8 Marks)**

   (c) Write a short note on multiprocessor and multi computers. **(6 Marks)**

2. (a) Explain various types of rotate instructions **(6 Marks)**

   (b) Explain the features of RISC processor. **(8 Marks)**

   (c) Write the instruction format MOV AX CX instruction. **(6 Marks)**

3. (a) What are condition code flags? Explain the use of them. **(6 Marks)**

   (b) Explain basic instruction types with the help of examples. **(4 Marks)**

   (c) What is an addressing modes? Explain different types of addressing modes. **(10 Marks)**

4. (a) Draw and explain the timing diagram for modified synchronous input data transfer with multiple clock cycles. **(6 Marks)**

   (b) Which type of I/O devices are interfaced through DMA? Explain the bus-arbitation process used for DMA? **(10 Marks)**

   (c) Give comparison between memory mapped I/O and I/O mapped I/O. **(4 Marks)**

5. (a) Explain various types of SCSI bus termination. **(5 Marks)**

   (b) Explain the features of USB. **(5 Marks)**

   (c) Describe SDRAM and DDR SDRAM operations for data transfer between main memory and cache memory system. **(10 Marks)**

6. (a) In a two level virtual memory, $tA_1 = 10^{-7}$ and $tA_2 = 10^{-2}S$. What must be the hit ratio 'H' in order for the access efficiency to be atleast 90 percent of its maximum possible value. **(5 Marks)**

Contd.... 2

(b) Compare flash drives with hard disk drives. **(5 Marks)**

(c) Draw the disk controller interface connection and explain the major functions of disk controller. **(10 Marks)**

7. (a) Write a short note on look ahead carry generator. **(5 Marks)**

(b) Explain how Booths algorithm is suitable for signed number multiplication in comparison of conventional shift and add method. **(10 Marks)**

(c) Draw and explain typical hardwired control unit. **(5 Marks)**

8. (a) Draw and explain the multiple bus organisation. Explain its advantages. **(10 Marks)**

(b) With a block diagram, explain the operation of a digital camera? **(10 Marks)**

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CS/IS46

USN | | | | | | | | | | |

NEW SCHEME

Fourth Semester B.E. Degree Examination, July 2006
EC/TE/EE/IT/ML/BM/CS/IS
Computer Organization

Time: 3 hrs.] [Max. Marks:100

Note: *1. Answer any FIVE full questions.*
2. Answer should be brief and to the point.

1 a. Distinguish between :
i) Pipelining and super scalar operation
ii) CISC and RISC
iii) Multiprocessors and multicomputers. **(09 Marks)**

b. Explain clearly SPEC Rating and its significance. **(03 Marks)**

c. Convert the following pairs of numbers to 5 bit signed 2's complement binary numbers and add them. State whether an overflow occurs in each case.
i) -14 and 11 ii) -10 and -13. **(04 Marks)**

d. Discuss the two ways in which byte addresses are assigned across words. **(04 Marks)**

2 a. Explain with a specific example how a stack frame is built and dismantled for a particular invocation of a subroutine. **(08 Marks)**

b. Which of the following possibilities for saving return address of a subroutine support subroutine nesting and which support subroutine recursion and why?
i) in a processor register ii) in a memory location associated with call
iii) on a stack. **(04 Marks)**

c. Explain clearly the Bus Arbitration Methods. **(08 Marks)**

3 a. Draw a combined input / output interface circuit and explain the different operations clearly. **(10 Marks)**

b. Consider a synchronous bus that transfers data in one clock cycle. Address transmitted by the processor appears on the bus after 4 nanoseconds, propagation delay on the bus varies from 1 to 5 nanoseconds, address decoding takes 6 nanoseconds. Addressed device takes 5 to 10 nanoseconds to place the data on the bus. Input buffer needs 3 nanoseconds setup time. Estimate the clock speed at which this bus can operate. **(04 Marks)**

c. Distinguish between the processor clock speed and bus clock speed and explain why the disparity occurs between the two. State the values of the above in a modern computing system. **(06 Marks)**

4 a. Discuss the main phases involved in the operation of SCSI bus in detail. **(10 Marks)**

b. Explain the operation of a split bus with a diagram. **(05 Marks)**

c. With a diagram explain USB packet format clearly. **(05 Marks)**

Contd... 2

5 a. Draw a block diagram for 8m X 32 memory system using 512 k X 8 memory chips and explain its operation. **(08 Marks)**

b. Discuss direct mapped, associative mapped and set associative mapped CACHE memory system with suitable diagrams. **(08 Marks)**

c. Define Hit Rate and Miss Penalty. **(04 Marks)**

6 a. Show the organization of a typical associative mapped TLB and explain how address truncation takes place. **(10 Marks)**

b. Explain the organization and how data is accessed from a disk. State the typical values for recording surfaces, tracks, sectors, bytes / sectors, access time in a disk. **(10 Marks)**

7 a. Discuss the Booth's Multiplication Algorithm with an example. **(10 Marks)**

b. With a clear diagram explain the floating point addition – subtraction unit. **(10 Marks)**

8 a. With a diagram which shows the separation Decoding and Encoding functions. Explain hard wired control **(10 Marks)**

b. With a block diagram explain an embedded processor with all the salient blocks and their functions. **(10 Marks)**

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CS46

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NEW SCHEME

Fourth Semester B.E. Degree Examination, Dec. 06 / Jan. 07
CS / IS / EC / TE / EE / IT / ML / BM
Computer Organisation

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Briefly explain the history of computer development from first generation to fourth generation computers. **(08 Marks)**

b. Quoting an example for each explain :
   i) Different types of instructions in a computer to perform various operations.
   ii) Different addressing modes used to specify the location of operand.
   found in most computers. **(09 Marks)**

c. List three important differences between how a stack and a queue are organized. **(03 Marks)**

2 a. Convert the following pairs of decimal numbers to 5-bit, signed, 2's complement binary numbers and add them. State whether or not overflow occurs in each case.
   i) 7 and 13
   ii) –5 and 7
   iii) –14 and 11
   iv) –10 and -13 **(08 Marks)**

b. With the help of suitable examples, illustrate encoding of machine instructions. **(12 Marks)**

3 a. For a simple example of I/O operations involving a keyboard and a display device, write a assembly language program that reads one line from the keyboard, stores it in memory buffer and echoes it back to the display. **(08 Marks)**

b. In a situation where number of operationally independent devices capable of initiating interrupts are connected to a processor, what are the different challenges faced by the processor? How does the processor take care of these challenges? **(12 Marks)**

4 a. Showing the possible register configurations in a DMA interface, explain direct memory access. **(08 Marks)**

b. Considering the timing diagrams, explain the sequence of events for input transfer and output transfer on a synchronous bus. **(08 Marks)**

c. List out the functions of an I/O interface. **(04 Marks)**

5 a. With the block diagram explain the operation of a 16-megabit DRAM chip configured as 2M×8.

b. Which are the various factors to be considered in the choice of a memory chip? Explain.

c. Give the organization of a 2M×32 memory module using 512k×8 static memory chips.

Contd.... 2

6 a. Write a note on flash memory. **(06 Marks)**

b. Is the average access time experienced by the processor an excellent indicator of the effectiveness of a particular implementation of the memory hierarchy? Explain. **(08 Marks)**

c. With a block diagram explain the virtual memory organization. **(06 Marks)**

7 a. A half adder is a combinational logic circuit that has two inputs, x and y and two outputs, s and c, that are the sum and carry-out respectively, resulting from the binary addition of x and y.

i) Design a half adder as a two-level AND-OR circuit.

ii) Show how to implement a full-adder using two half-adder and external logic gates as necessary.

iii) Compare the longest logic delay path through the network derived in part (ii) to that of the logic delay of the adder network implemented using basic gates. **(05 Marks)**

b. Illustrate with an example the algorithm for non restoring binary division. **(08 Marks)**

c. Write IEEE standard floating-point formats for 32-bit representation and explain. **(07 Marks)**

8 a. With the control sequence for the instruction add R_4, R_5, R_6, explain the three-bus organization of data path in a processor. **(08 Marks)**

b. Explain microinstruction sequencing with next address field. **(06 Marks)**

c. Explain the example of embedded system in a digital camera. **(06 Marks)**

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CS46

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NEW SCHEME

Fourth Semester B.E. Degree Examination, July 2007
CS / EC / EE / IS / TE / IT
Computer Organization

Time: 3 hrs.] [Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Explain different functional units of a computer. Mention the function of the processor registers i) PC ii) MAR iii) IR **(08 Marks)**

b. What is a bus? Explain single bus and multiple bus structure used to interconnect functional units in computer system. **(08 Marks)**

c. Explain with an illustration multitasking. **(04 Marks)**

2 a. Explain how the performance of a computer can be measured. What are the measures to improve the performance of computers? **(06 Marks)**

b. Explain with illustration, the three systems of representing binary numbers, which system is most often used in computers? **(06 Marks)**

c. What is overflow in integer arithmetic? Explain how overflow can be detected, with an illustration. **(08 Marks)**

3 a. Explain

i) Byte addressability ii) Big-endian assignment iii) Little endian assignment. **(06 Marks)**

b. Mention four types of operations required to be performed by instruction in a computer. What are the basic types of instruction formats? Give an example for each. **(08 Marks)**

c. What do you mean by addressing mode? Explain any four addressing modes. Give one example for each type. **(06 Marks)**

4 a. Compare CISC and RISC systems. **(04 Marks)**

b. With neat block diagram, explain any two methods of handling multiple I/O devices. **(08 Marks)**

c. What is the necessity of DMA controller? Explain the methods of bus arbitration. **(08 Marks)**

5 a. What are functions of an I/O interface? Explain with a block diagram I/O interface between a keyboard and a processor. **(06 Marks)**

b. Explain serial port and a serial interface. **(05 Marks)**

c. What is USB? What are the objectives of USB? Explain USB architecture. **(09 Marks)**

6 a. Mention any two differences between static and dynamic RAMs. Explain the internal organization of a memory chip consisting of 16 words of 8 bit each. **(06 Marks)**

b. Explain with block diagram and timing diagram synchronous DRAM. **(08 Marks)**

c. What is secondary storage? Explain in brief magnetic hard disk. **(06 Marks)**

7 a. How do you design FAST ADDERS? Explain a 4 bit carry look ahead adder. **(06 Marks)**

b. Explain the sequential binary multiplier with the use of a block diagram. **(06 Marks)**

c. Explain the computational details of multiplying two 4 bit numbers 1 0 1 1 and 0 1 0 1 using Booths algorithm. Verify the result obtained. **(08 Marks)**

8 a. With a block diagram explain the general requirements of a microwave oven or a digital camera in embedded systems. **(10 Marks)**

b. Explain the concept of micro programmed control unit. **(10 Marks)**

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CS46

Fourth Semester B.E. Degree Examination, Dec. 07 / Jan. 08
Computer Organization

Time: 3 hrs. Max. Marks:100

Note : ***Answer any FIVE full questions.***

1 a. Describe the basic functional units of a computer using a schematic. **(10 Marks)**

b. Program execution time is defined by T = N*S/R. A program can be run on a RISC or a CISC computer. Both computers use pipelined instruction execution. Effective value of S in T for RISC machine is 1.2 but it is only 1.5 for CISC machine. Both machines have the same clock rate R. Find the value of N on the CISC machine as a percentage of N for the RISC machine if the time for execution on both the machines is the same. Recalculate the ratio if the clock rate R for the RISC machine is 15% higher than for the CISC machine. **(05 Marks)**

c. Explain the following with reference to 2's compliment arithmetic:
i) Sign extension ii) Arithmetic overflow. **(05 Marks)**

2 a. Write an assembly language program to add a list of numbers using indirect addressing. **(08 Marks)**

b. Explain the concept of stack frames when subroutines are nested. **(06 Marks)**

c. The return address of a subroutine could be saved: i) In a processor register ii) In a memory location associated with the call so that a different location is used when the subroutine is called from the different places iii) On a stack.
Which of the above mentioned possibilities supports subroutine nesting and which supports subroutine recursion? **(06 Marks)**

3 a. What is the need for disabling interrupts? What are the different ways in which interrupts can be disabled and enabled? **(08 Marks)**

b. Draw neat timing diagrams and explain: i) Multicycle synchronous bus transfer for a read operation ii) Asynchronous bus transfer for a write operation. **(12 Marks)**

4 a. Three devices A, B and C are connected to the bus of a computer. I/O transfers for all three devices use interrupt control. Interrupt nesting for devices A and B is not allowed. But interrupt requests from C may be accepted while either A or B is being serviced. Suggest different ways in which this can be accomplished in the following cases:
i) The computer has one interrupt request line ii) Two interrupt request lines INTR1 and INTR2 are available with INTR1 having higher priority.
Specify when and how interrupts are enabled and disabled in each case. **(05 Marks)**

b. Explain the different phases in the operation of the SCSI bus. **(10 Marks)**

c. Draw the block diagram of a 8Mx32 memory using 512Kx8 memory chips. **(05 Marks)**

5 a. Explain the working of a dynamic memory cell. **(05 Marks)**

b. Explain how an address generated by the processor gets translated into a main memory address. **(10 Marks)**

c. A block-set-associative cache consists of a total of 64 blocks divided into 4-block sets. The main memory contains 4096 blocks each consisting of 128 words.
i) How many bits are there in the main memory address?
ii) How many bits are there in each of the TAG, SET and WORD fields? **(05 Marks)**

6 a. Explain the circuit arrangement that implements restoring division. **(06 Marks)**

b. Let multiplicand A = 110101 and multiplier B = 011011. Multiply the given signed 2's compliment numbers using booth algorithm. Verify the result using bit pairing of the multiplier. **(06 Marks)**

c. Let floating point numbers be represented in a 12-bit format consisting of one bit for the sign, five bits for excess-15 exponent with two end values 0 and 31 signifying 0 and infinity respectively and six bits for the fractional mantissa normalized as in the IEEE format with an implied 1 to the left of the binary point.
i) Represent 12.125 in this format.
ii) What are the smallest and largest numbers that can be represented in this format? **(08 Marks)**

7 a. Draw a neat block diagram and explain the single bus organization. **(10 Marks)**

b. List out the advantages and limitations of a hard-wired control unit. Explain the organization of a micro-programmed control unit. **(10 Marks)**

8 Write notes on: **(10 Marks)**

a. USB architecture b. Compact Disk (CD) technology c. Digital camera as an example of an embedded system d. Carry look-ahead addition. **(20 Marks)**

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06CS46

Fourth Semester B.E. Degree Examination, Dec.08 / Jan.09
Computer Organization

Time: 3 hrs. Max. Marks:100

Note : ***Answer FIVE full questions, selecting at least two questions from each Part A and Part B.***

Part A

1 a. Explain the different functional units of a computer with a neat block diagram. **(10 Marks)**

b. Write the basic performance equation. Explain the role of each of the parameters in the equation on the performance of the computer. **(05 Marks)**

c. Represent the number 81234561 in 32-bit Big-endian and little-endian memory organization. **(05 Marks)**

2 a. What is the need for an addressing mode? Explain the following addressing modes with examples: immediate, direct, indirect, index, relative. **(07 Marks)**

b. What is subroutine linkage? How are parameters passed to subroutines? **(06 Marks)**

c. What is a stack frame? Explain. **(07 Marks)**

3 a. Discuss the different schemes available to disable and enable interrupts. **(06 Marks)**

b. How are simultaneous interrupt from more than one devices handled? **(06 Marks)**

c. What does the term "cycle steating" mean? **(02 Marks)**

d. Write a note on any one bus arbitration scheme. **(06 Marks)**

4 a. Draw and explain the block diagram of a typical serial interface. How does it compare with a parallel interface? **(10 Marks)**

b. Explain the main phases involved in SCSI bus operation. **(10 Marks)**

Part B

5 a. Differentiate between SRAM and DRAM. **(02 Marks)**

b. Sketch and explain the internal organization of a 2M×8 dynamic memory chip. **(07 Marks)**

c. Explain any one cache mapping function. **(05 Marks)**

d. A computer has byte addressable memory with a cache that can hold eight 32-bit words. Each cache block consists of one 32-bit word. The following sequence of hex addresses are read during program execution:
200, 204, 208, 2OC, 2F4, 2FO, 200, 204, 218, 21C, 24C, 2F4
Assuming that the cache is initially empty, show the contents of the cache if
i) direct mapping is used ii) associative mapping with LRU replacement is used. **(06 Marks)**

6 a. Draw a block diagram and explain how a virtual address from the processor is translated into a physical address in the main memory. **(05 Marks)**

b. Write notes on: i) Optical technology used in CD systems ii) RAID Disk arrays. **(08 Marks)**

c. Draw a figure to illustrate and explain a 16-bit carry look ahead adder using 4-bit adder blocks. Show that the carry and sum are generated in 5 and 8 gate delays respectively. **(07 Marks)**

7 a. Draw the hardware implementation of Booth's multiplication algorithm. **(04 Marks)**

b. Trace the steps in the above implementation to multiply –5 ×–4. **(05 Marks)**

c. Illustrate the steps for non-restoring division algorithm on the following data: dividend = 1011, divisor = 0101. **(05 Marks)**

d. If A and B are two single precision floating point numbers where
A = 44900000H and B = 42A00000H
Show the results of (A+B) and (A-B). **(06 Marks)**

8 a. Draw a figure of the single bus organization of the processor unit. **(04 Marks)**

b. List the actions needed to execute the instruction Add R1, (R3). Write the sequence of control steps to perform the actions for a single bus structure. Explain the steps. **(10 Marks)**

c. Compare hardwired control unit with micro programmed control unit. **(06 Marks)**

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06CS46

Fourth Semester B.E. Degree Examination, Dec.09/Jan.10
Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. With a neat diagram, explain in detail the functional units of a computer. **(10 Marks)**

b. How the performance of a computer is measured? Assuming that the reference computer is Ultra SPARCIO workstation with 300MHz Ultra SPARC-IIi processor. A company has to purchase 500 new computers, hence ordered testing of a new computer with SPEC2000 (run on reference as well as new computer). Following observations were made.

Programs	Runtime on reference computer	Runtime in new computer
1	50 Minutes	5 Minutes
2	75 Minutes	4 Minutes
3	60 Minutes	6 Minutes
4	30 Minutes	3 Minutes

The company's system manager will place the orders for purchasing new computers only if the overall SPEC rating is at least 12.00. After the said test, will the system manager place order for the purchase of new computers? **(10 Marks)**

2 a. Convert the following pairs of decimal numbers to 5 bit signed 2's complement binary numbers and add them. Also state whether overflow occurs in each case.
i) -5 & 7 ii) -3 & -8 iii) -10 & -13. **(06 Marks)**

b. Write a program which evaluates the expression A×B+C×D in a single accumulator processor. Assume that processor has load, store, multiply and add instructions and all the values fit in the accumulator. **(05 Marks)**

c. Explain how the parameters are passed to a subroutine? Write a program to multiply a list of 'n' numbers stored in memory, which calls a subroutine namely, LISTMUL and trace the program with suitable example. **(09 Marks)**

3 a. In modern computers, why interrupts are required? Support your claim with a suitable example. **(06 Marks)**

b. In the interrupt mechanism, how the simultaneous arrivals of interrupts from various (multiple) devices (I/O) are handled? **(06 Marks)**

c. With neat sketches, explain the various approaches to bus arbitration. **(08 Marks)**

4 a. With a neat sketch, explain the individual input and output interface circuits. Also elicit their salient features. **(10 Marks)**

b. In a computer system, why a PCI Bus is used? With a neat sketch, explain how the read operation is performed, along with the role of IRDY# / TRDY#, on the PCI Bus. **(10 Marks)**

PART – B

5 a. Draw a diagram and explain the working of a 16 mega bit DRAM chip configured as 2M×8. Also explain as to how it can be made to work in fast page mode. **(10 Marks)**

b. Assume that a computer has L1 and L2 caches. The cache blocks consist of 8 words. Assume that the hit rate is same for both caches and that it is equal to 0.95 for instructions and 0.90 for data. Assume also that the times needed to access an 8-word block in these caches are C_1=1 cycle and C_2 = 10 cycles, then answer the following:

i) What is the average access time experienced by the processor if the main memory uses interleaving where the memory access parameters have usual meaning (M=17 with interleaving & M=38 without interleaving, assume that 30% of the instructions in a typical program perform a read or write operations). **(04 Marks)**

ii) What is the average access time if the main memory is not interleaved? **(04 Marks)**

iii) What is the improvement obtained through interleaving? **(02 Marks)**

6 a. Explain in detail, the working principle of a magnetic hard disk. **(10 Marks)**

b. A disk unit has 24 recording surfaces. It has a total of 14,000 cylinders. There are an average of 400 sectors per track. Each sector contains 512 bytes of data. Answer the following questions.

i) What is the maximum no. of gigabytes that can be stores in this unit? **(04 Marks)**

ii) What is the data transfer rate in bytes/sec at a rotational speed of 7200 rpm? **(03 Marks)**

iii) Using a 32-bit word, suggest a suitable scheme for specifying the disk address, assuming that there are 512 bytes/sector. **(03 Marks)**

7 a. Draw circuit diagram for binary division. Explain the restoring and non-restoring division algorithms with suitable examples. **(10 Marks)**

b. Explain the concept of carry save addition for the multiplication operation, M×Q=P for 4-bit operands, with diagram & suitable example. **(10 Marks)**

8 a. Explain the process of fetching a word from memory using timing diagram of memory read operation. Also give an example for the same. **(10 Marks)**

b. Write the control sequence of execution of the instruction ADD (R3), R1. For this sequence of instructions the processor is driven by a continuously running clock such that each control step is 2 ns in duration. How long will the processor have to wait in steps 2 & 5, assuming that a memory read operation takes 16 ns to complete? Also compute the percentage of time for which the processor is idle during the execution of this instruction. **(10 Marks)**

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06CS46

Fourth Semester B.E. Degree Examination, June-July 2009
Computer Organization

Time: 3 hrs. Max. Marks:100

Note: ***Answer any FIVE full questions, selecting at least TWO questions from each part.***

PART – A

1 a. Explain the function of processor registers with a block diagram. **(08 Marks)**

b. Write the basic performance equation. Explain the role of each of the parameters in the equation on the performance of the computer. **(07 Marks)**

c. Show how the operation C = A + B can be implemented in a single accumulator computer by (i) Three-address instruction (ii) Two-address instruction (iii) One-address instruction **(05 Marks)**

2 a. What is an addressing mode? Explain register, indirect, index addressing modes with an example for each. **(08 Marks)**

b. What is subroutine linkage? Explain with an example, subroutine linkage using linkage register. **(07 Marks)**

c. Register R1 and R2 of computer contain the decimal value 1200 and 4600. What is the effective address of the source operand in each of the following instructions?

i) Load 20(R1), R5
ii) Hove # 3000, R5
iii) Store R5, 30(R1, R2)
iv) Add -(R2), R5
v) Subtract (R1)+, R5

(05 Marks)

3 a. Explain with a diagram, how interrupt request from several I/O devices can be communicated to a processor through a single INTR line. **(08 Marks)**

b. How can the processor obtain the starting address of different interrupt-service routines using vectored interrupts? **(04 Marks)**

c. Why is bus arbitration required? Explain with block diagram bus arbitration using Daisy chain. **(08 Marks)**

4 a. Explain with a block diagram a general 8 bit parallel interface. **(08 Marks)**

b. With the help of data transfer signals explain how a real operation is performed using PCI bus. **(08 Marks)**

c. Explain briefly bus arbitration phase in SCSI bus. **(04 Marks)**

PART – B

5 a. Draw the organization of a 1K × 1 memory cell and explain its working. **(08 Marks)**

b. Explain the working of a single-transistor dynamic memory cell. **(07 Marks)**

c. Calculate the average access time experienced by a processor if a cache bit rate is 0.88, miss penalty is 0.015 milliseconds and cache access time is 10 microseconds. **(05 Marks)**

6 a. Show the organization of virtual memory address translation based in fixed-length pages and explain its working. **(08 Marks)**

b. How can performance and reliability be improved using RAID technology? **(04 Marks)**

c. Explain the design of a 4-bit carry-look ahead adder. **(08 Marks)**

7 a. Explain Booth's algorithm. Multiply 01110 (+14) and 11011 (-5) using Booth's multiplication. **(10 Marks)**

b. Write the algorithm for binary division using restoring division method. **(04 Marks)**

c. List the rules for addition, subtraction, multiplication and division of floating point numbers. **(06 Marks)**

8 a. Write and explain the control sequences for execution of an unconditional branch instruction. **(10 Marks)**

b. Explain with block diagram the basic organization of a microprogrammed control unit. **(08 Marks)**

c. What are the modifications required in the basic organization of a microprogrammed control unit to support conditional branching in the microprogram. **(02 Marks)**

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